


LCFC Confidential

PICASSO EX95 Rev1.0 Schematic

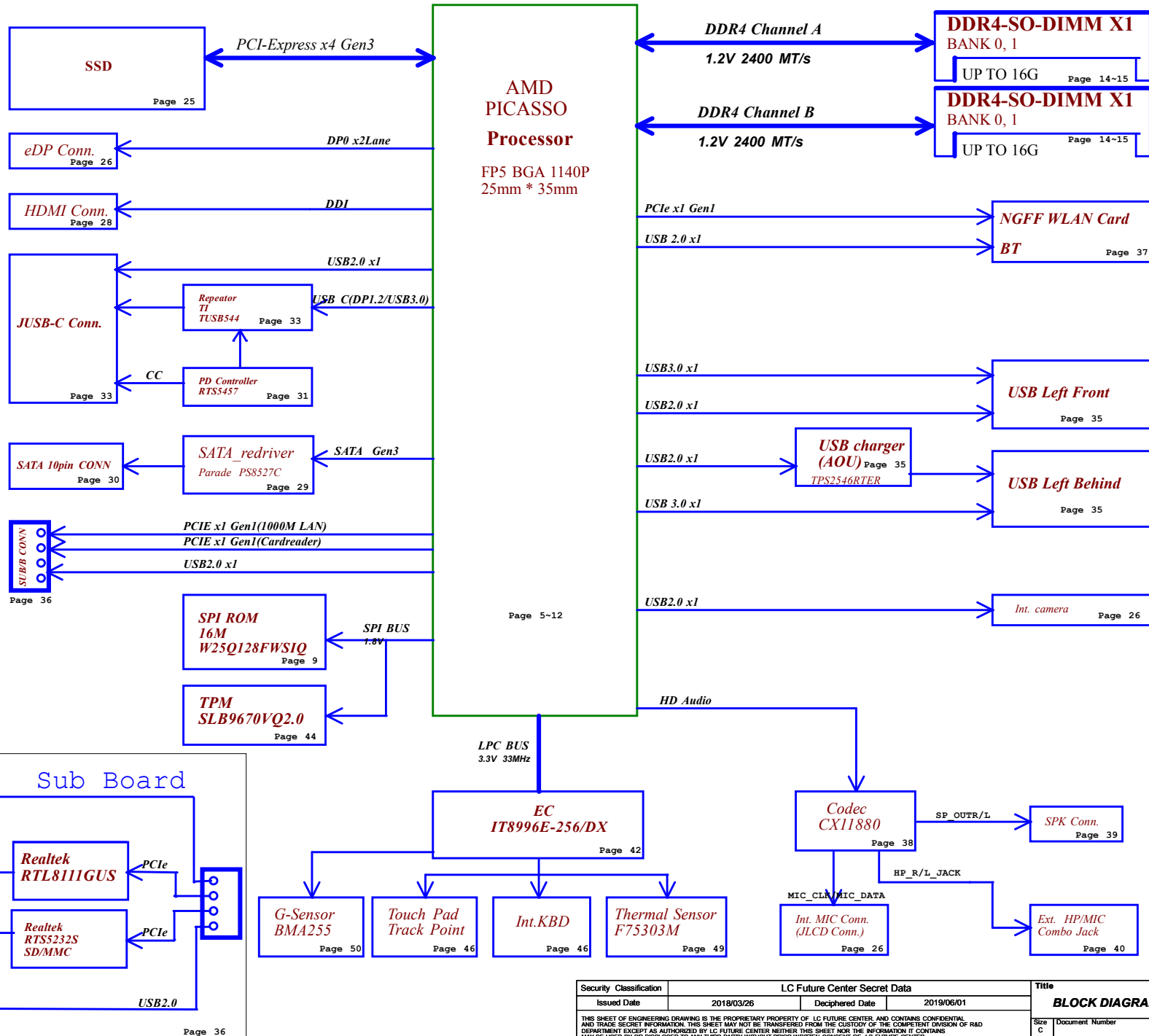
AMD Picasso FP5 Processor with DDR4

2019-01-08 Rev1.0

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AMD Raven Ridge FP5



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane				+5VS +3VS +1.8VS +0.9VS_VDDP +0.6VS +VDDCR_SOC +VDDC_VDD +VGA_CORE
State	B9+	+3VALW +5VALW +1.8VALW +0.9VALW_VDDP	+1.2V +2.5V	
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SUSP#	SLP_S5#	SYSON	EC_ON	
S0		HIGH		HIGH		ON	
S3 (Suspend to RAM)		LOW		HIGH		ON	
S4 (Suspend to Disk)		LOW		LOW		ON	
S5 (Soft OFF)		LOW		LOW		ON	

USB2 Port

Port	Device
0	USBC
1	USB3 port1
2	USB3 port2
3	USB2 IOB
4	USB2 (BT)
5	Int. Camera

USB3 Port

Port	Device
0	USB Type-C
1	USB3 port1
2	USB3 port2
3	X
4	X

PCIE Port

Port	Device
GPP0	LAN
GPP1	CardReader
GPP2	X
GPP3	X
GPP4	WLAN
GPP5	X
GFX0	M.2 SSD
GFX1	M.2 SSD
GFX2	M.2 SSD
GFX3	M.2 SSD
GFX4~7	X

SATA Port

Port	Device
GPP6	SATA HDD
GPP7	X

SMBUS Control Table

EC	Schemic	SOURCE	DGPU	BATT	Charge	PMIC	PD	APU	G-Sensor	Thermal Sensor	SODIMM	CP Module
SMCLK1 SMDAT1	EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V +3VL	V +3VL	X	X	X	X	X	X	X
SMCLK0 SMDAT0	EC_SMB_CK2 EC_SMB_DA2	EC +3VL	X	X	X	X	V +3VL	X	X	X	X	X
SMCLK3 SMDAT3	EC_SMB_CK3 EC_SMB_DA3	EC +3VS	X	X	X	X	X	V +3VS	V +3VS	V +3VS	X	X
SMCLK2 SMDAT2	EC_SMB_CK4 EC_SMB_DA4	EC +3VL	X	X	X	V +3VL	X	X	X	X	X	X
	APU_SMB0CLK APU_SMB0DATA	APU +3VS	X	X	X	X	X	X	X	X	V +3VS	X
	APU_SMB1CLK APU_SMB1DATA	APU +3VALW	X	X	X	X	X	X	X	X	X	V +3VS

PD Controller I2C

	SOURCE	APU	Type C Redriver
REPETER_SCL REPETER_SDA	PD +LDO_3V3	V +1.8VALW	V +LDO_3V3



APPLY PCB PN



BOM Structure Table

BOM Structure	NOTE
HDT@	For HDT AMD debug port
LPC@	For LPC AMD debug port
TPM@	Trusted Platform Module (TPM)
UMA@	UMA SKU ID
CD@	COST DOWN
EMC_NS@	EMC Reserves
ME@	ME Connector
RF@	For RF function
EMC@	For EMI function
RF_NS@	reserves RF component

M.2 SSD

LAN

CardReader

WLAN

HDD

M.2 SSD

LAN

CardReader

WLAN

HDD

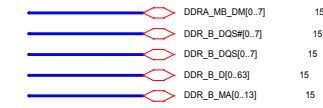
UC18

PCIe

PPS REV 030
PART 2 OF 13

AMD-RAVEN-PP5_BGA1140

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		2019/06/01		PCIE VF	
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UC1A

UC1I

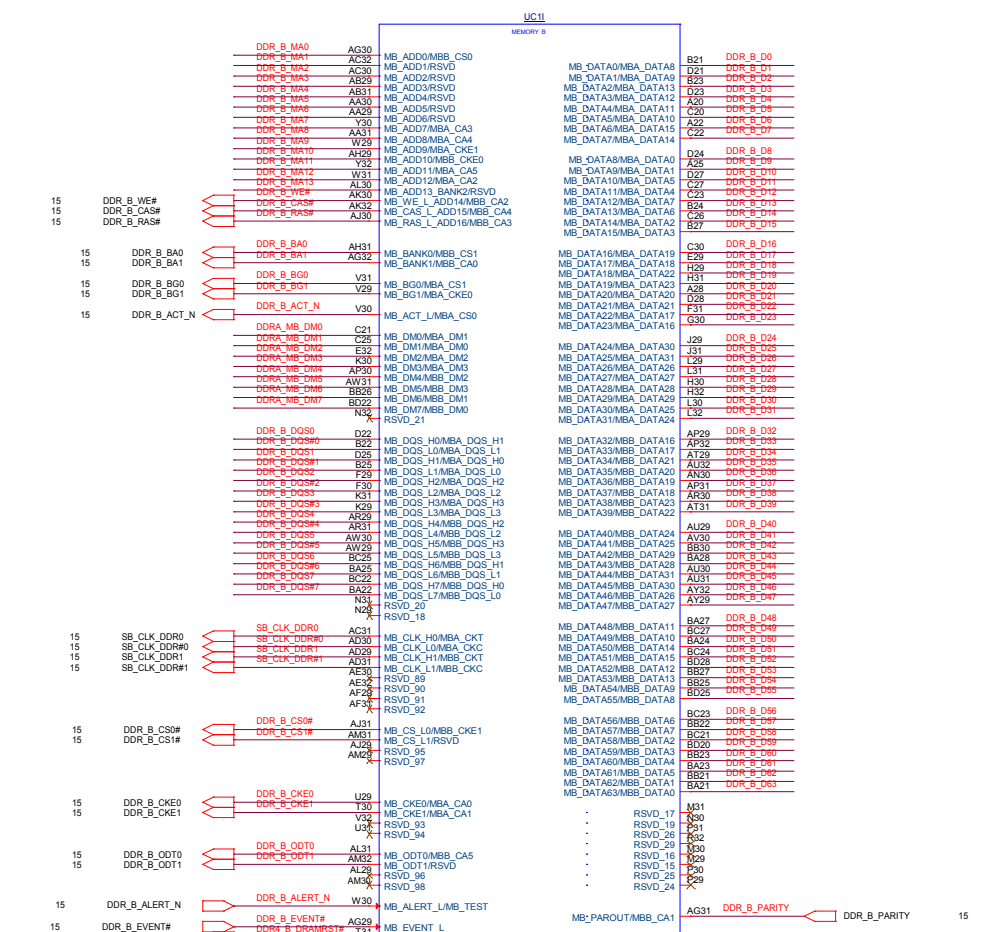
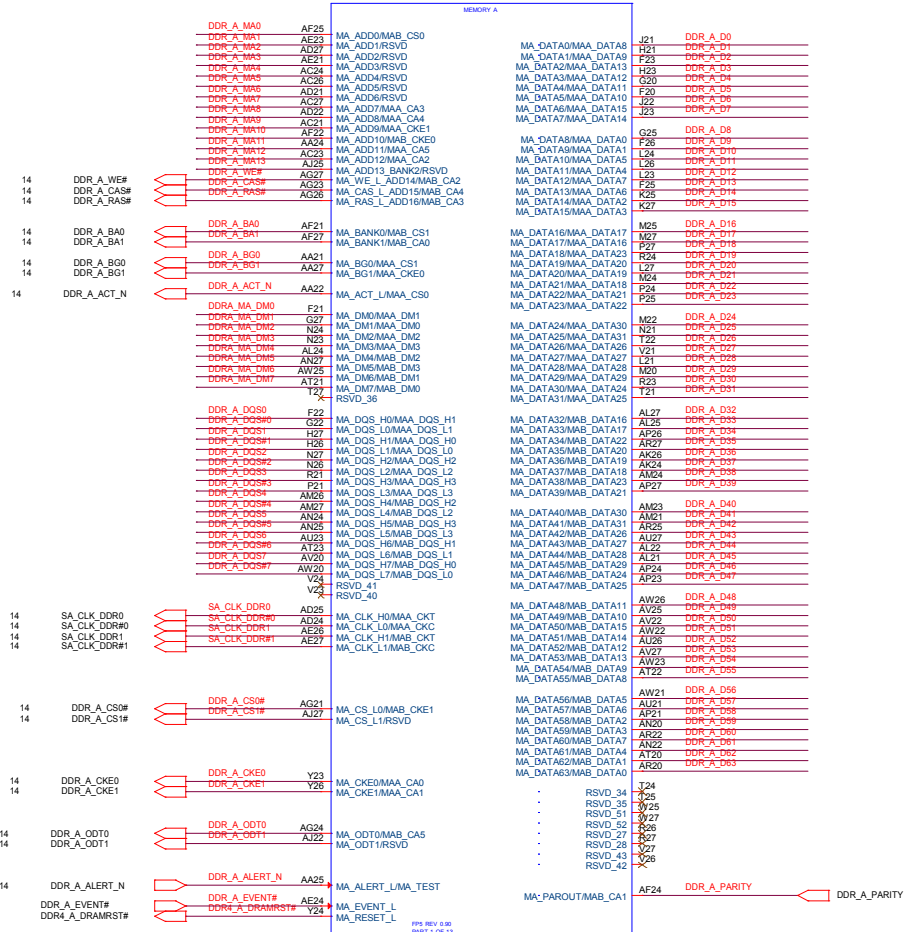
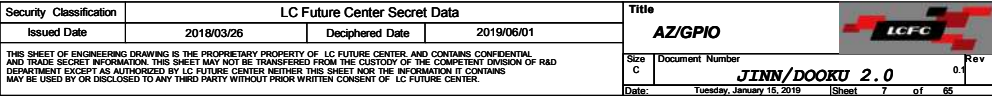


FIG. REV 0.00
PART 1 OF 13

FIG. REV 0.00
PART 2 OF 13

AMD-RAVEN-FP5_BGA1140



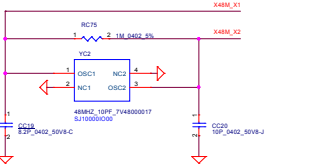
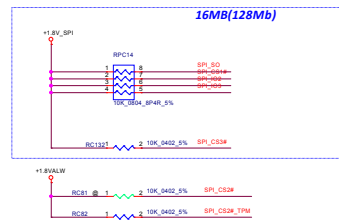


TABLE of Cystal (YC2)		
Vendor	LCFC P/N	Description
TXC	SJ10000IO00	S CRYSTAL 48MHZ 10PF +-20PPM 7V48000017
Siward	SJ10000M000	S CRYSTAL 48MHZ 10PF XTL571100-A31-076



LPC debug connector 20PIN, only reserve test point

As below is CRB circuit

LPC ROM EMULATOR HEADER

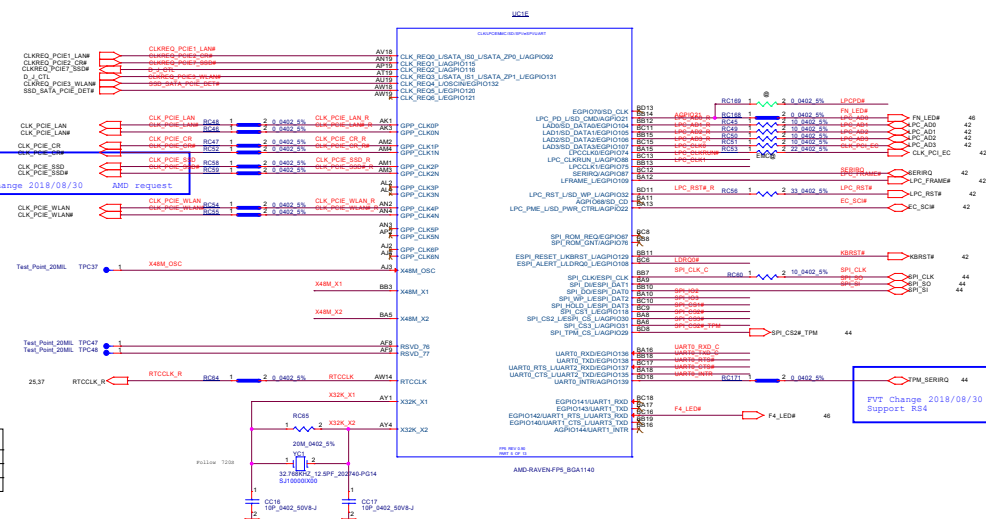
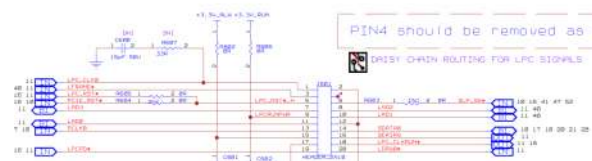
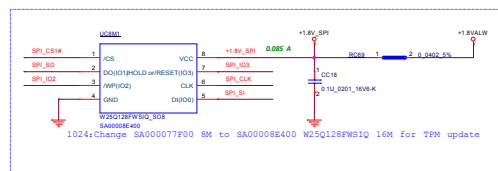
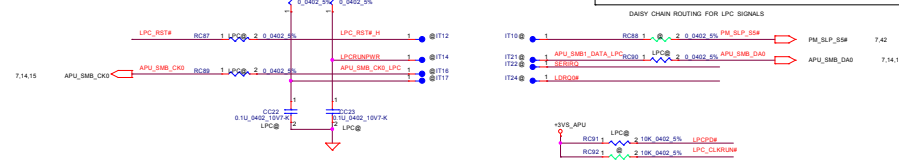


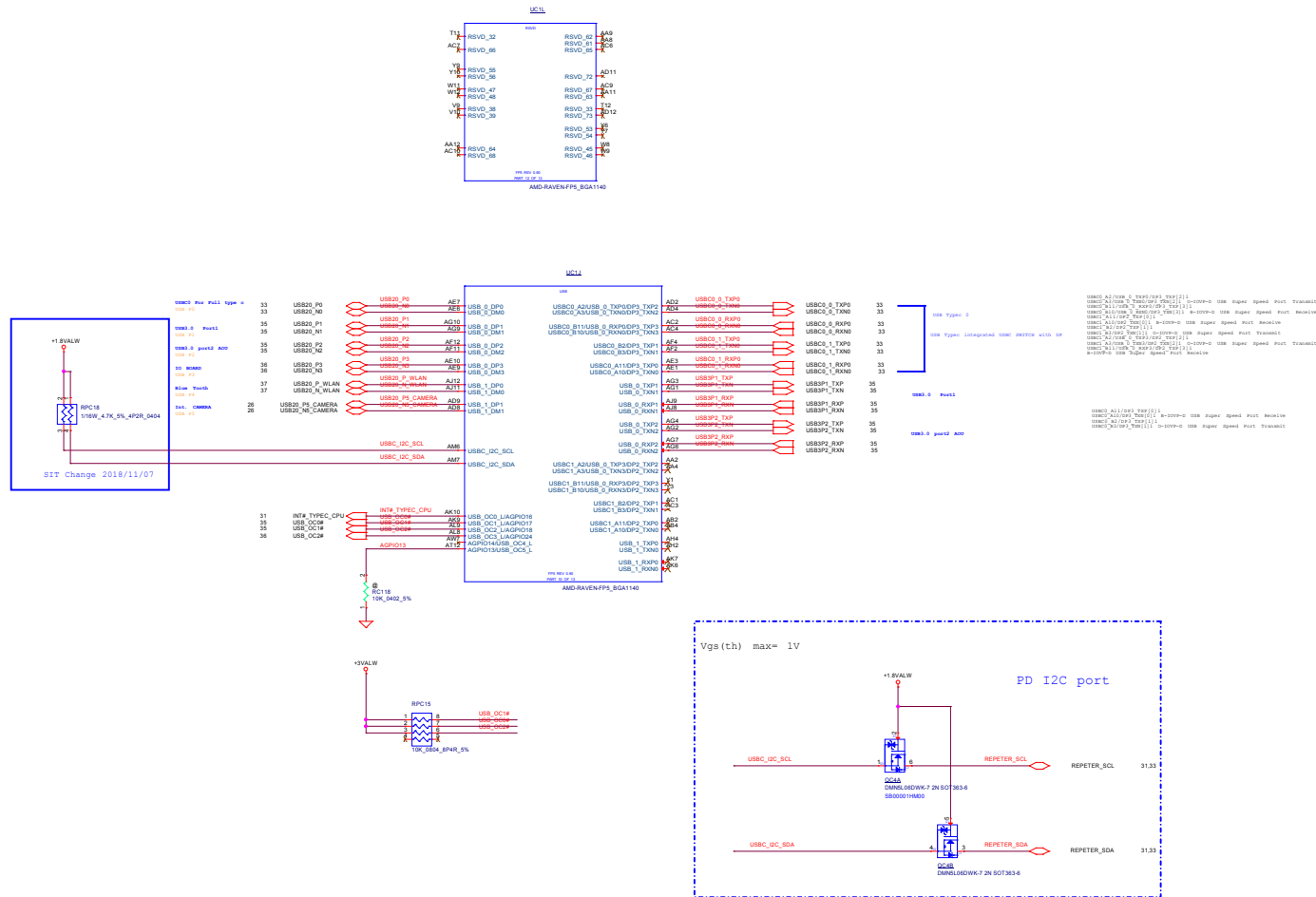
TABLE of Cystal (YC2)		
Vendor	LCFC P/N	Description
SEIKO	SJ10000IX00	S CRYSTAL 32.768KHZ 9PF X1A000141000200
SIWARD	SJ10000MU00	S CRYSTAL 32.768KHZ 9PF XTL721-L150-008

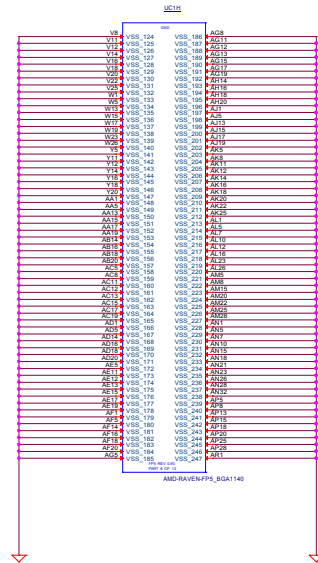
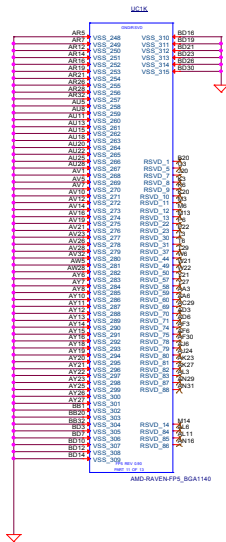
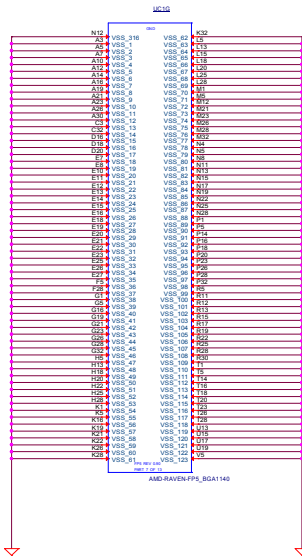


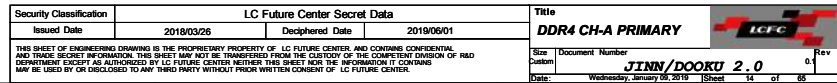
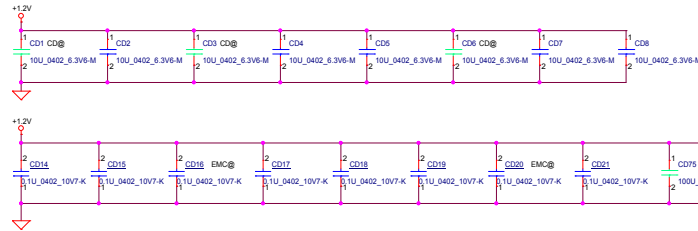
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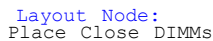
PIN4 should be removed as a Key




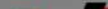


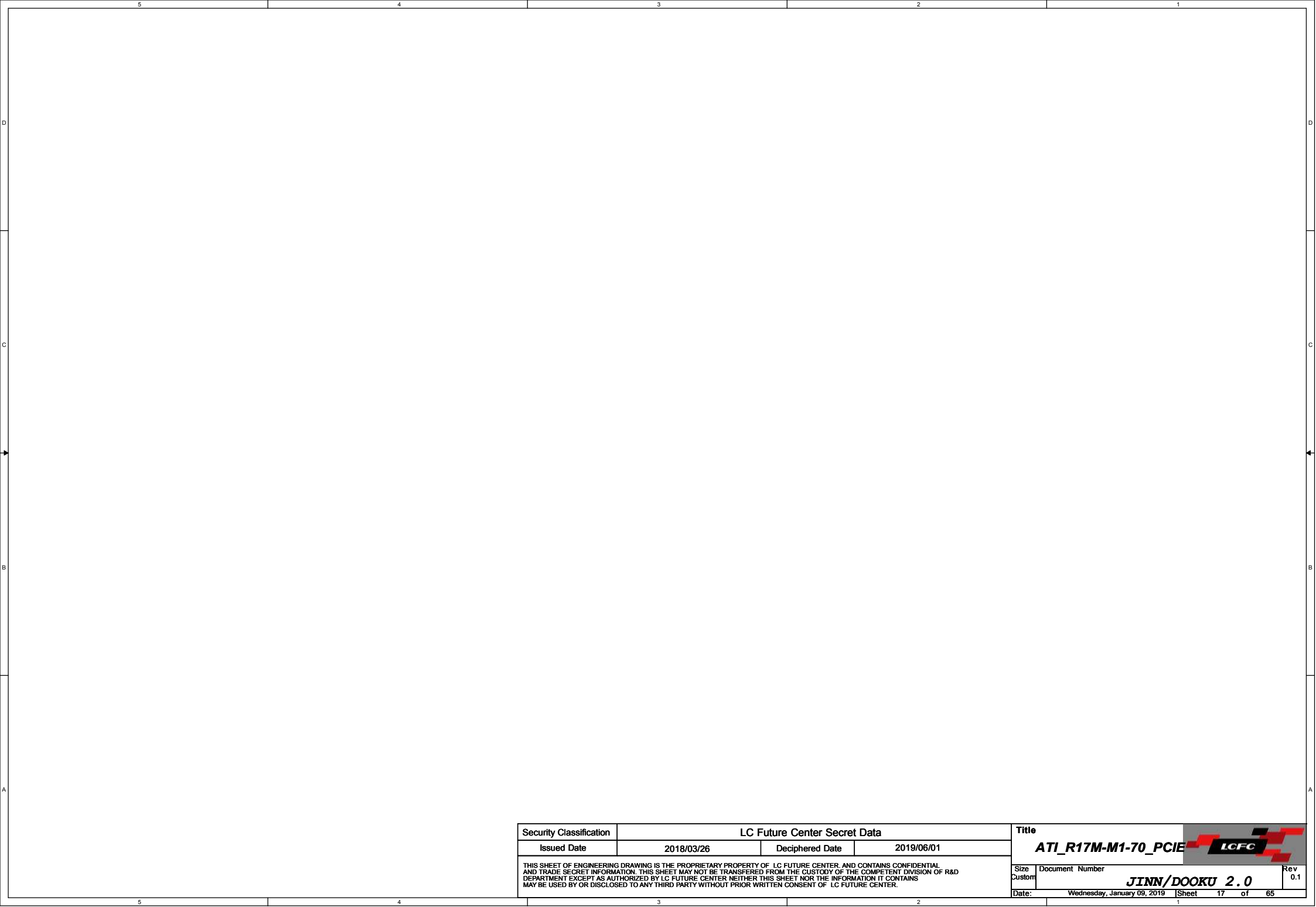







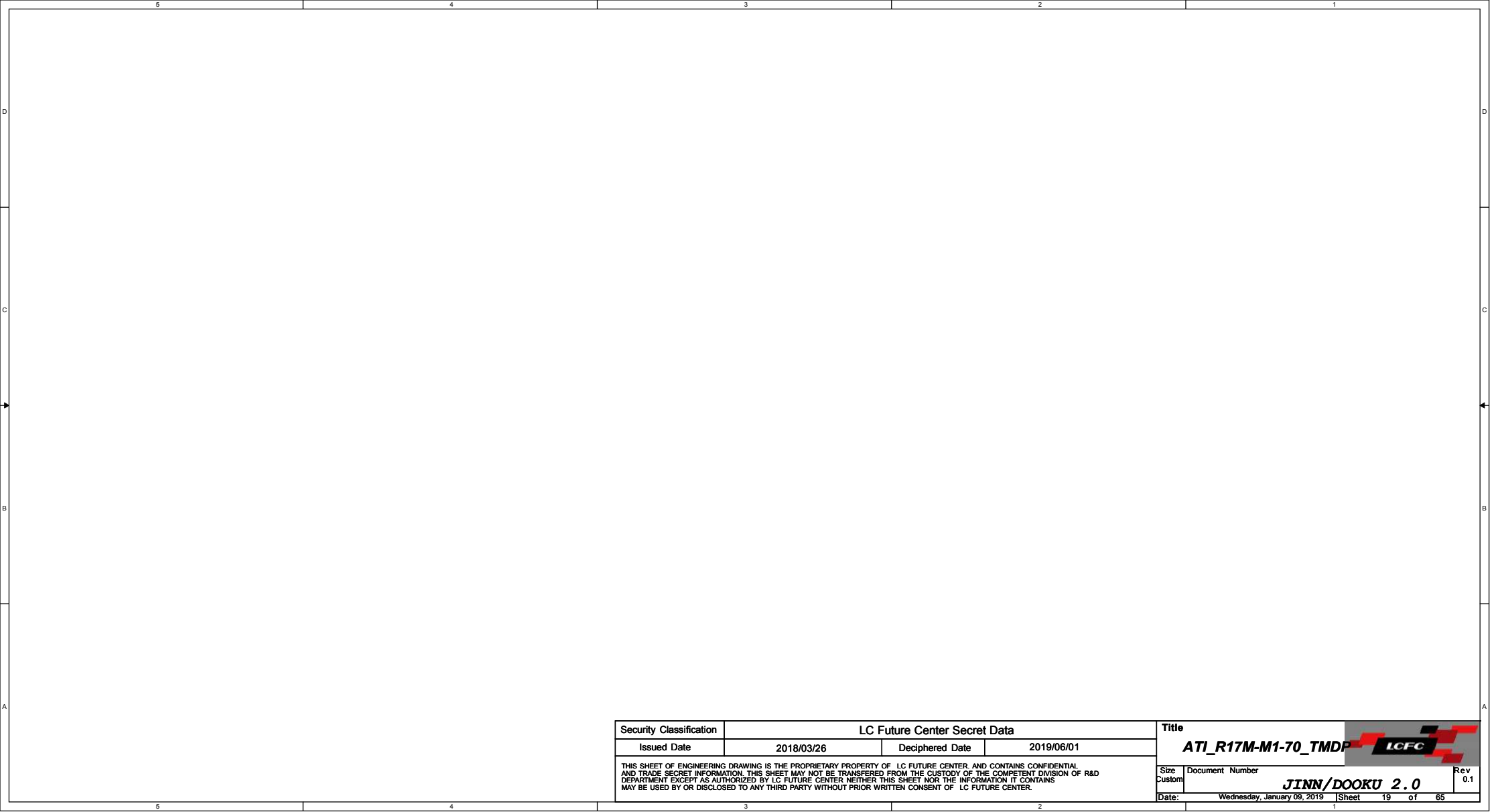
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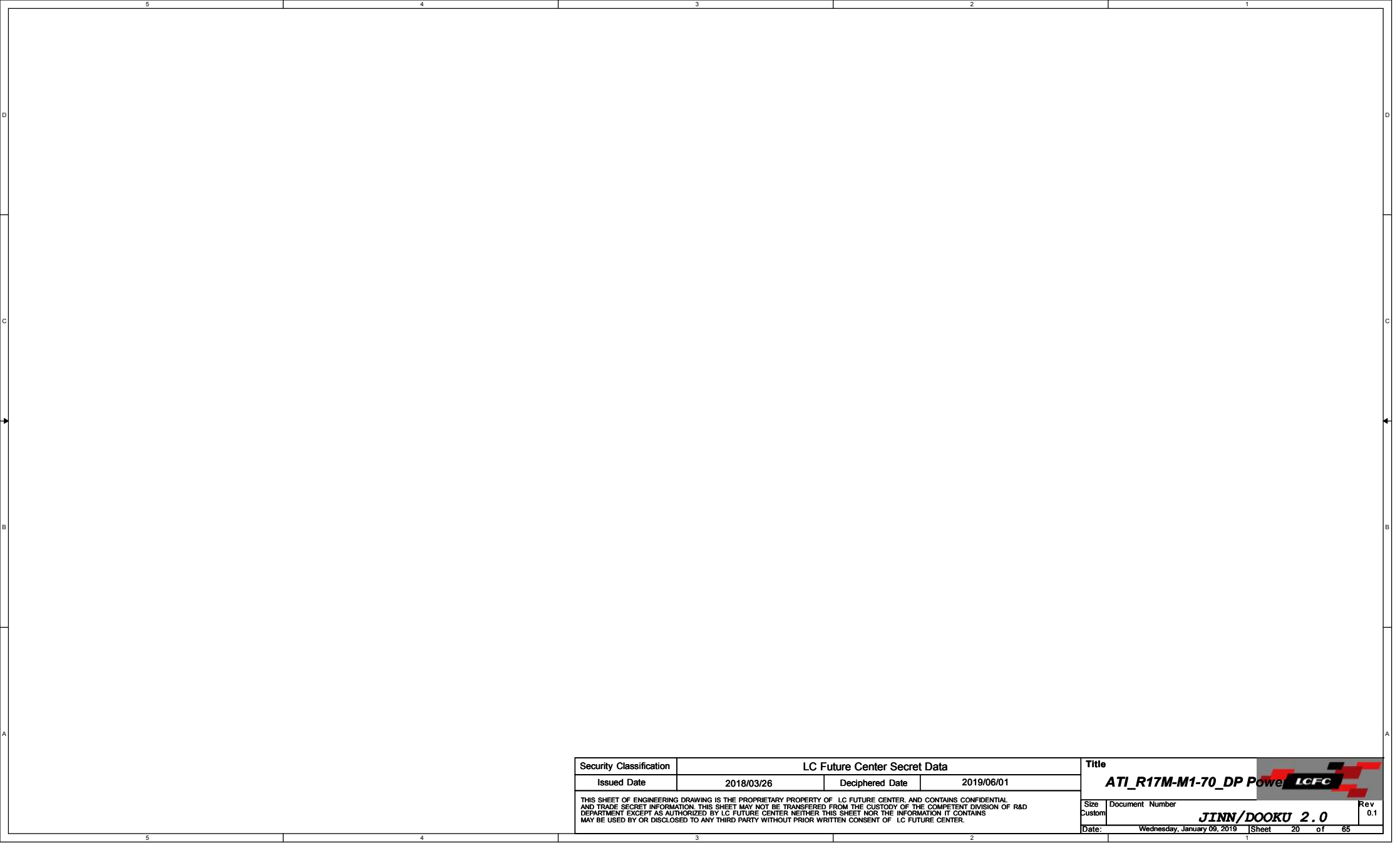



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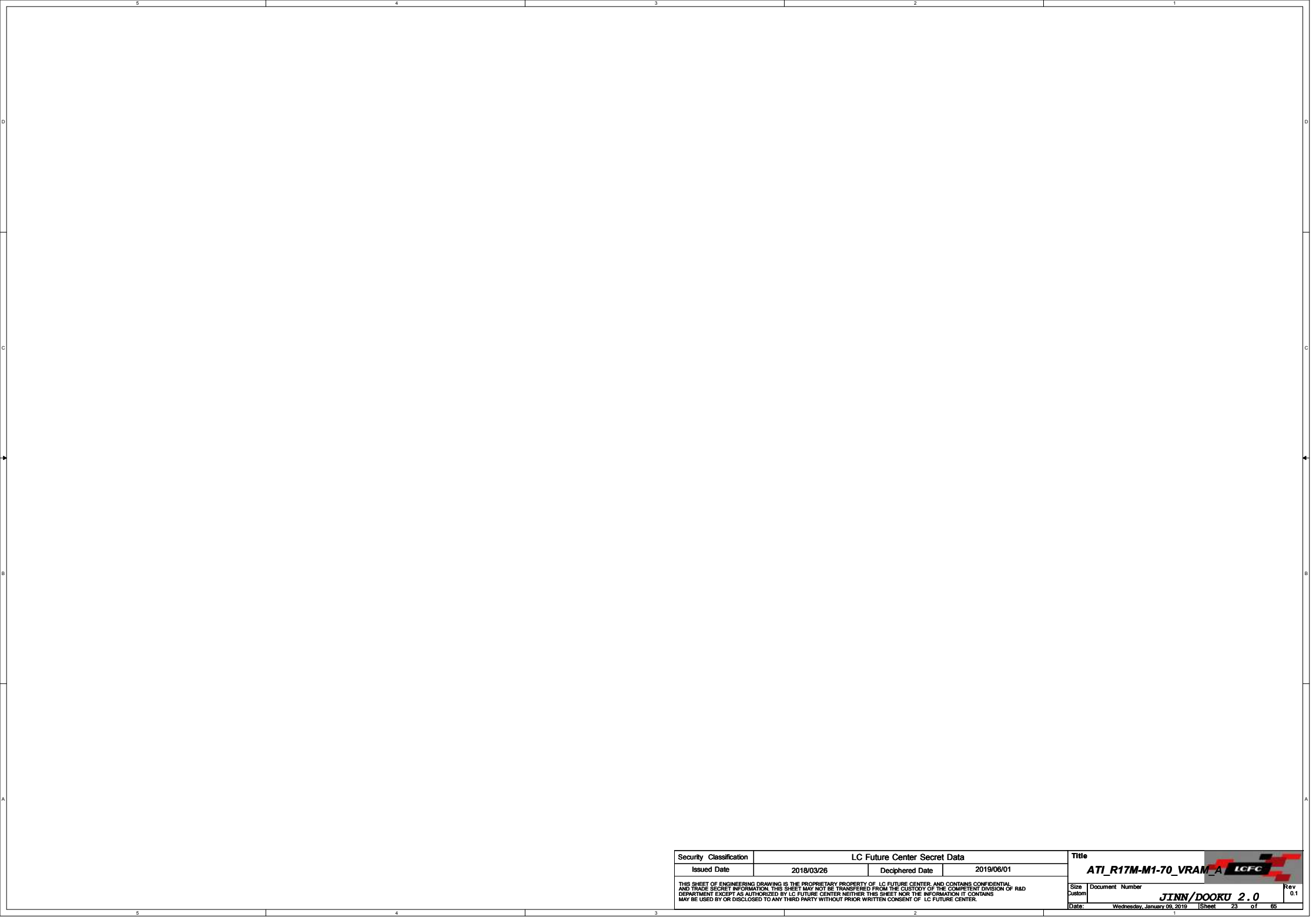
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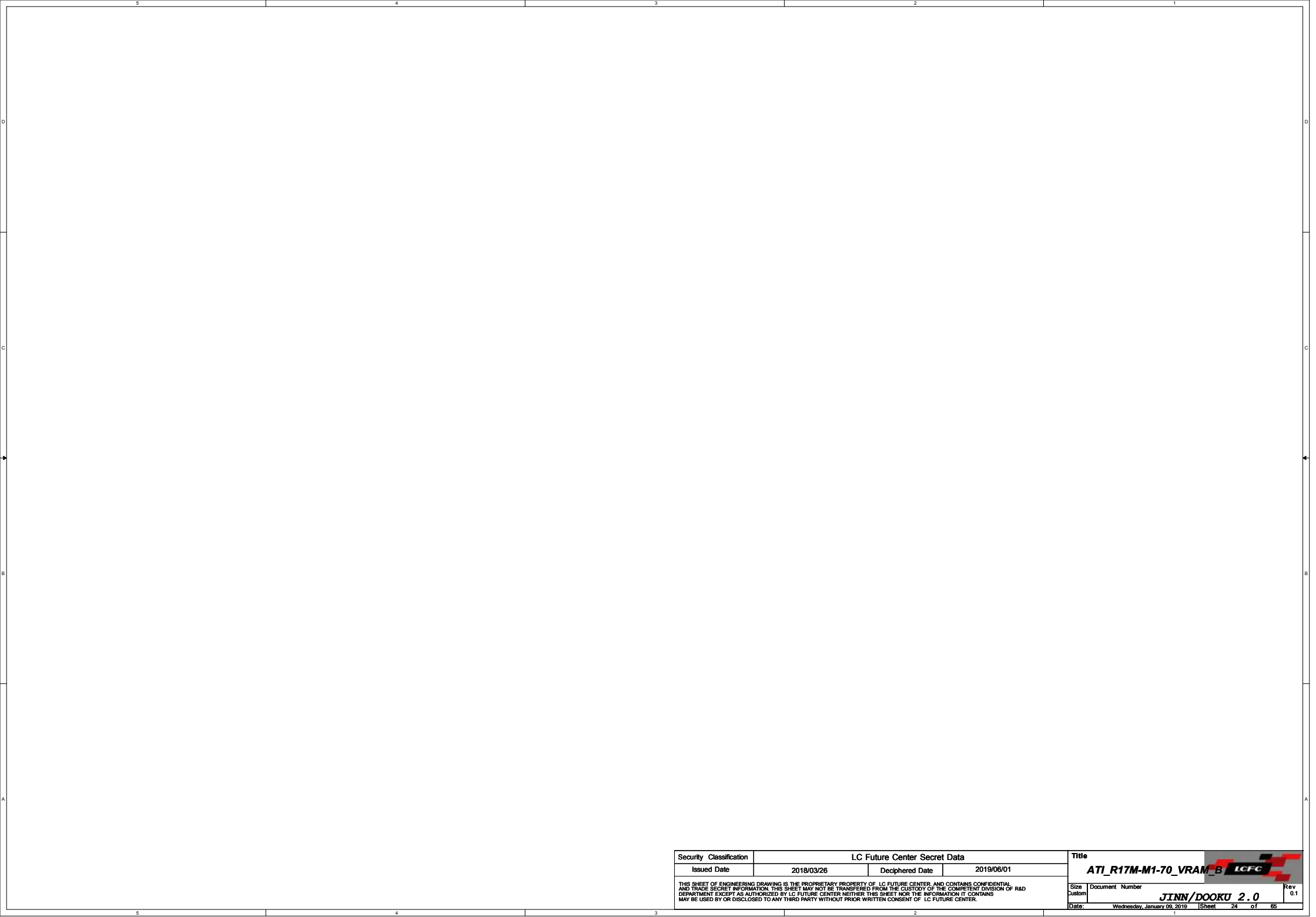
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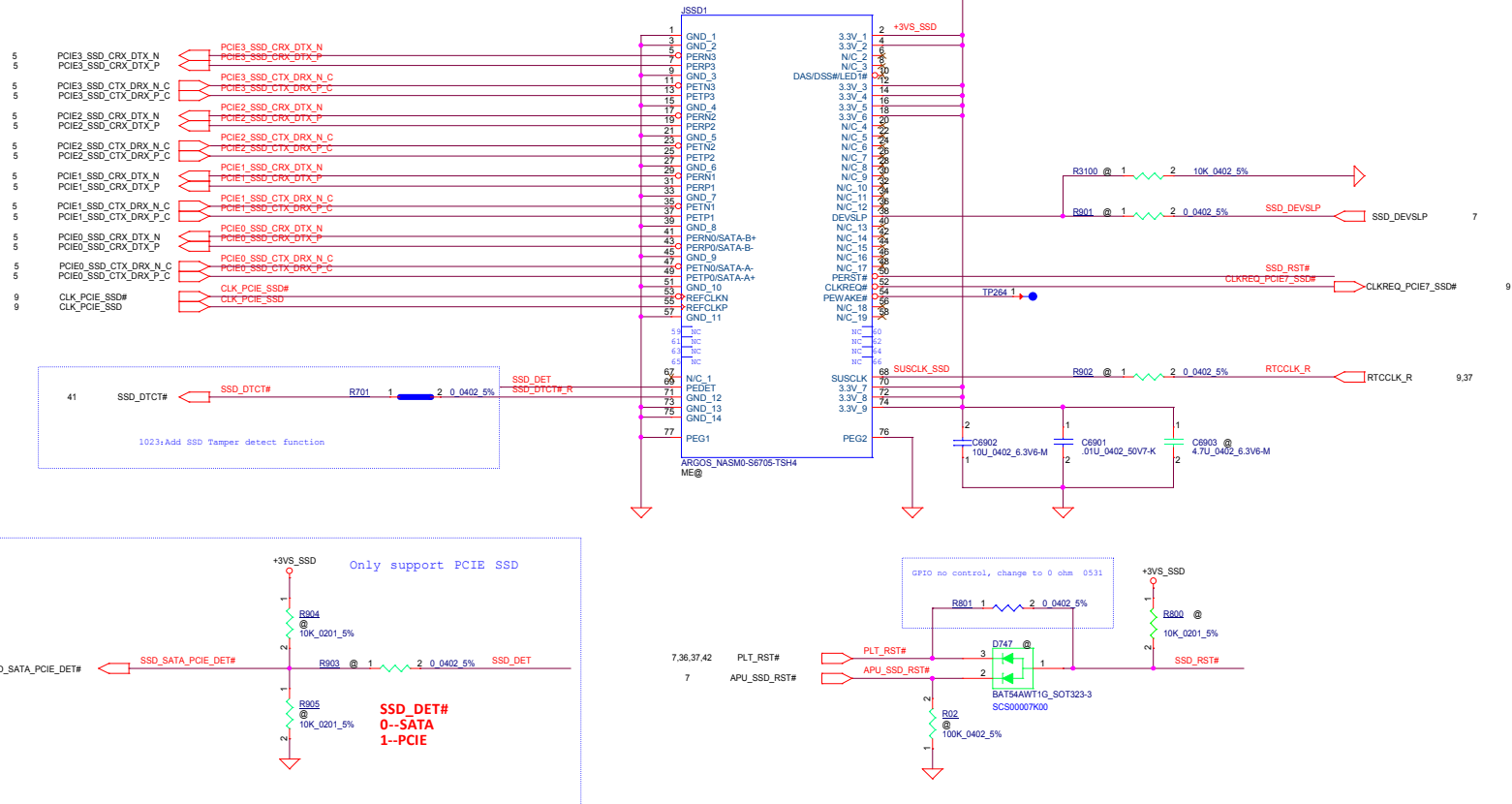
Table 35. Socket 3 PCIe-based Module Pinout

76	GPIO	GPIO	75
72	GPIO	GPIO	71
70	GPIO	GPIO	69
68	SUSCLK2M4M0 (M0/S, S0)	PEDET (INC/POW)	67
Module Key		Module Key	Module Key
Module Key		Module Key	
Module Key		Module Key	
Module Key		Module Key	
58	Reserved/AMPS Clock	GPIO	57
56	Reserved/AMPS Data	GPIO	55
54	PERWAKE0 (D0/D0/S, S0)	PERCLKIN	53
52	CLKREQ0 (D0/D0/S, S0)	GPIO	51
50	PERST0 (D0/D0/S, S0)	GPIO	49
48	N/C	PERWAKE0	47
46	N/C	GPIO	45
44	N/C	PETWAKE0	43
42	N/C	PERWAKE0	41
40	N/C	GPIO	39
38	DEVSUP (S)	PERWAKE0	37
36	N/C	PERWAKE0	35
34	N/C	GPIO	33
32	N/C	PETWAKE0	31
30	N/C	PERWAKE0	29
28	N/C	PERWAKE0	27
26	N/C	GPIO	25
24	N/C	PERWAKE0	23
22	N/C	GPIO	21
20	N/C	PERWAKE0	19
18	GPIO	PERWAKE0	17
16	GPIO	GPIO	15
14	GPIO	PERWAKE0	13
12	GPIO	PERWAKE0	11
10	GPIO	PERWAKE0	9
8	N/C	PERWAKE0	7
6	N/C	PERWAKE0	5
4	GPIO	GPIO	3
2	GPIO	GPIO	1

Table 32. Socket 2 PCIe-based SSD Module Pinout

76	GPIO	GPIO	75
72	GPIO	GPIO	71
70	GPIO	GPIO	69
68	SUSCLK2M4M0 (M0/S, S0)	CONFG1_1 = NC	67
Module Key		Module Key	Module Key
Module Key		Module Key	
Module Key		Module Key	
Module Key		Module Key	
58	Reserved for MFG Clock	GPIO	57
56	Reserved for MFG Data	GPIO	55
54	PERWAKE0 (D0/D0/S, S0)	PERCLKIN	53
52	CLKREQ0 (D0/D0/S, S0)	GPIO	51
50	PERST0 (D0/D0/S, S0)	GPIO	49
48	N/C	PERWAKE0	47
46	N/C	GPIO	45
44	N/C	PETWAKE0	43
42	N/C	PERWAKE0	41
40	N/C	GPIO	39
38	DEVSUP (S)	PERWAKE0	37
36	N/C	PERWAKE0	35
34	N/C	GPIO	33
32	N/C	PETWAKE0	31
30	N/C	PERWAKE0	29
28	N/C	PERWAKE0	27
26	N/C	GPIO	25
24	N/C	PERWAKE0	23
22	N/C	GPIO	21
20	N/C	CONFG1_0 = GND	19
Module Key		Module Key	Module Key
Module Key		Module Key	
Module Key		Module Key	
Module Key		Module Key	
10	GPIO	GPIO	9
8	N/C	GPIO	7
6	N/C	GPIO	5
4	GPIO	GPIO	3
2	GPIO	CONFG1_3 = GND	1

M.2 SSD(M TYPE)



LCDVDD Circuit

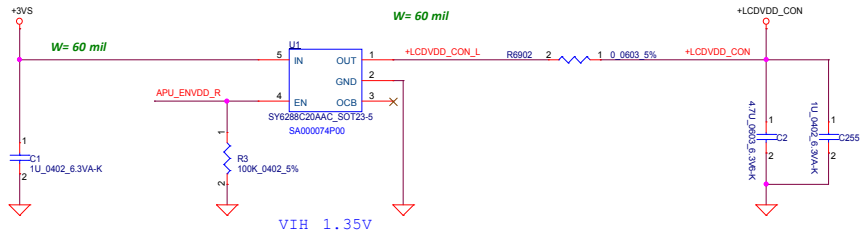
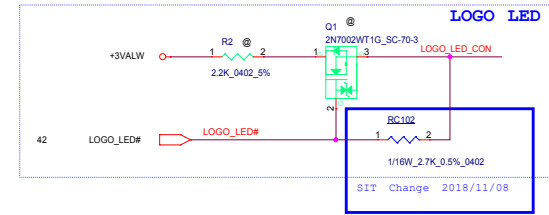
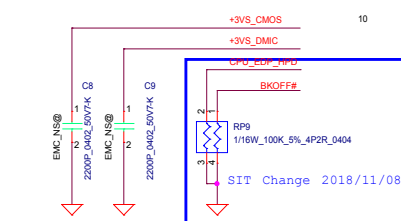
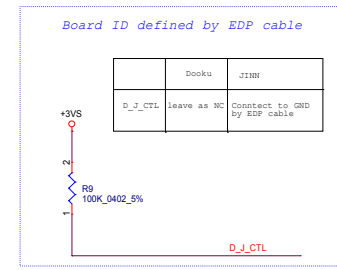


TABLE of POWER SWITCH (U1)

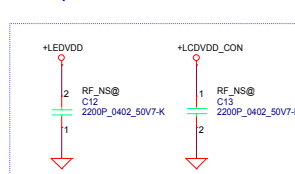
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GMT	SA00007S700	S IC G5247T11U SOT-23 5P POWER SWITCH



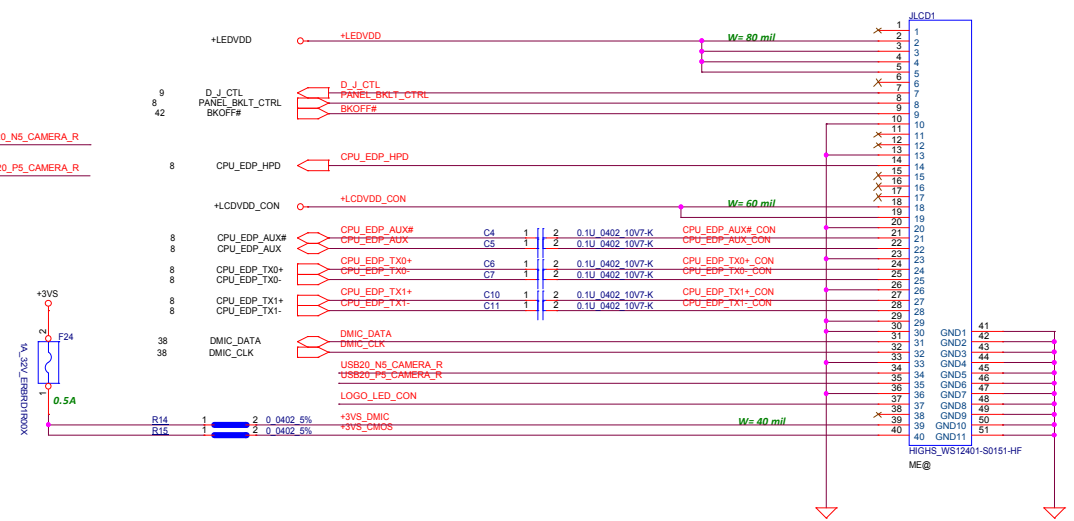
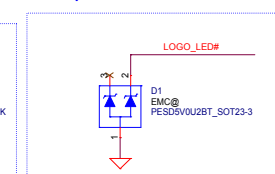
eDP/CMOS/LOGO-LED CONN.

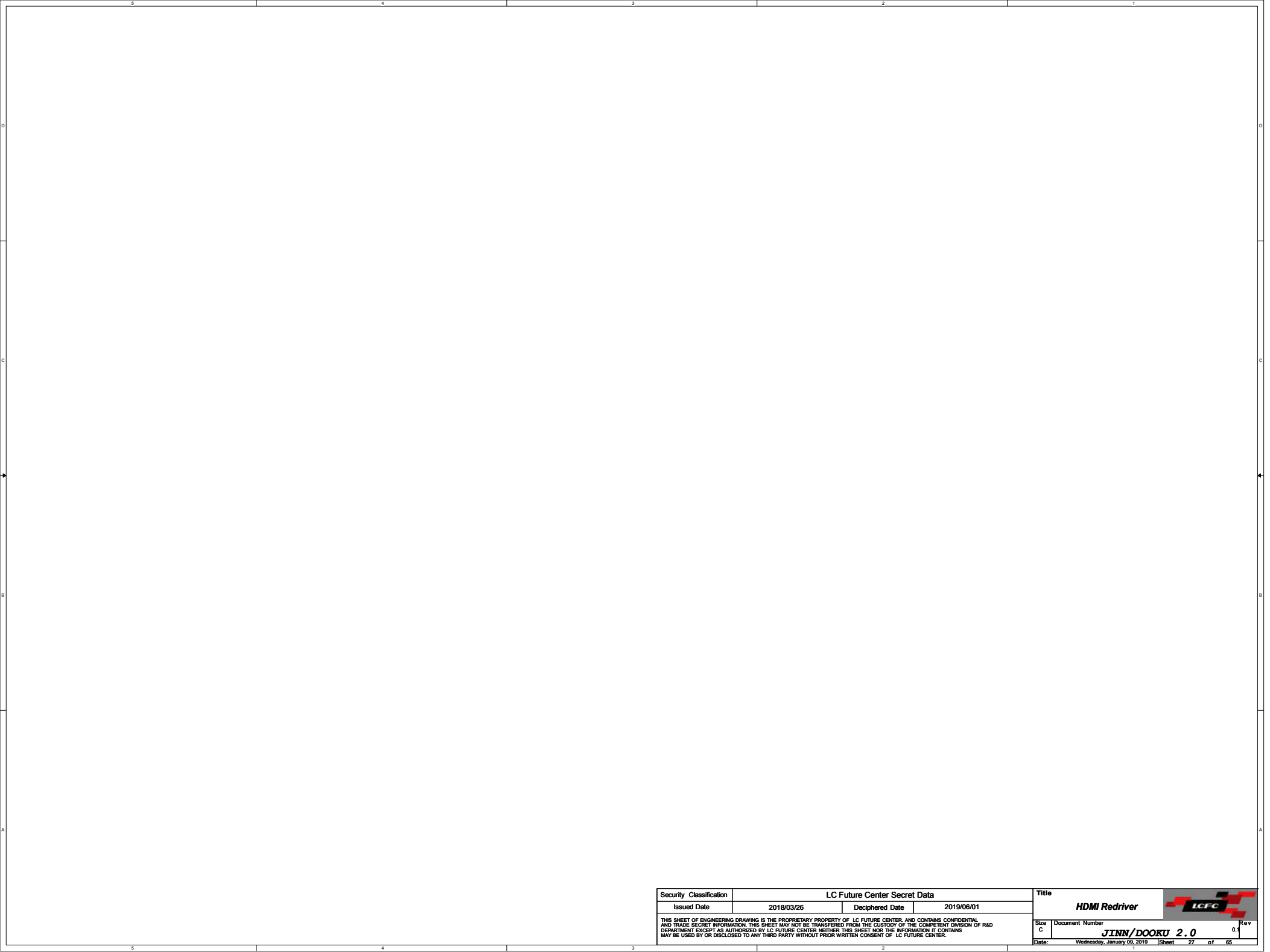


EMC request. Close to JLCD



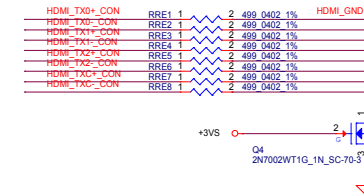
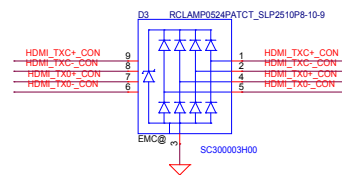
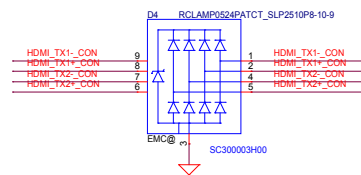
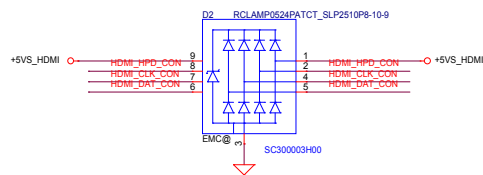
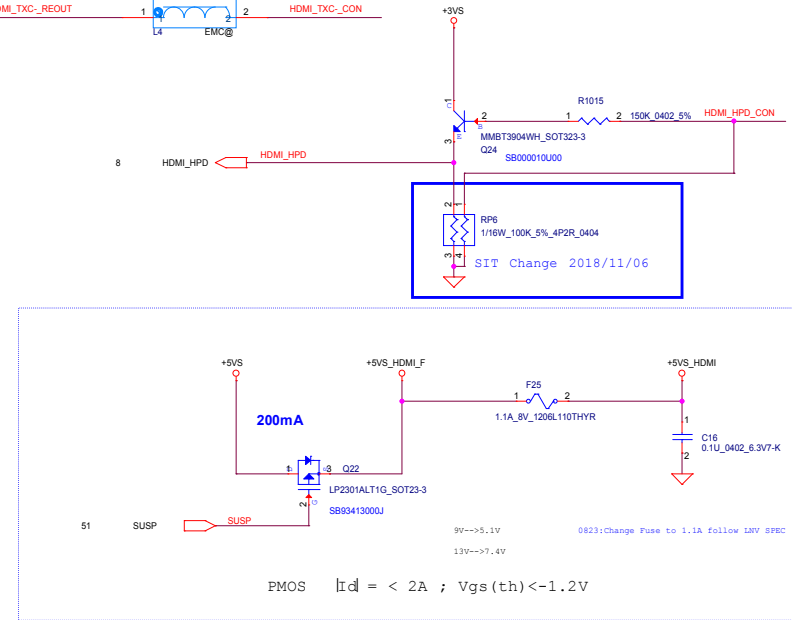
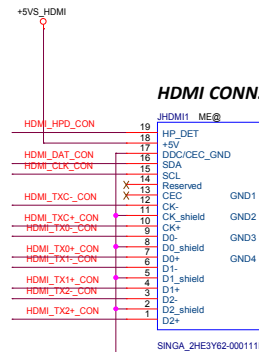
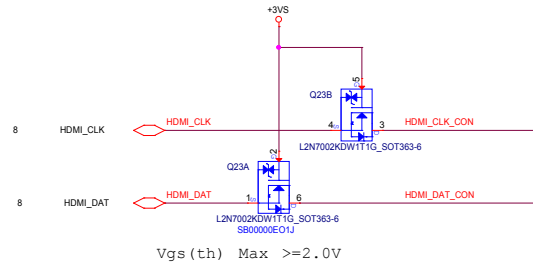
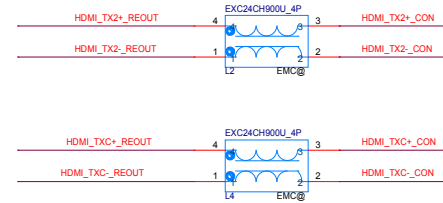
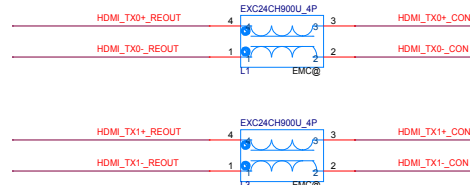
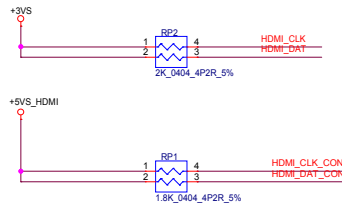
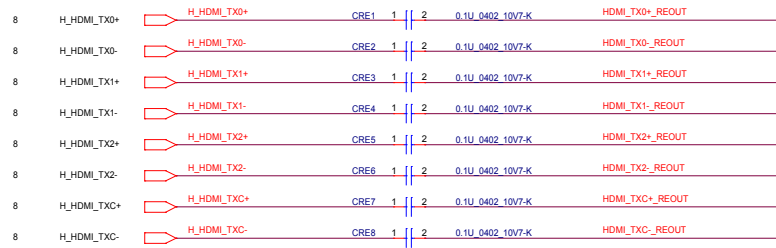
ESD request



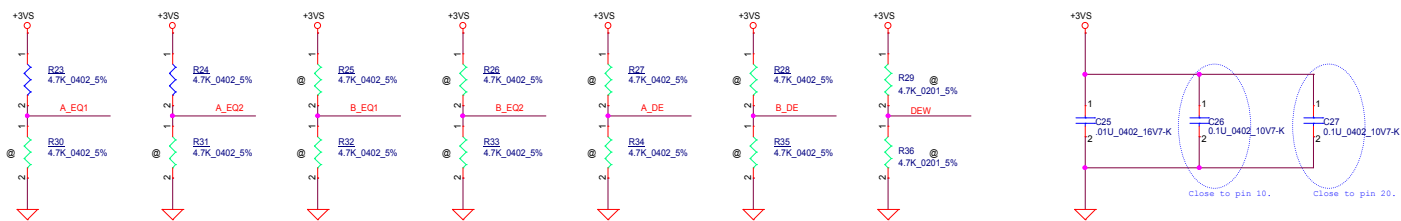
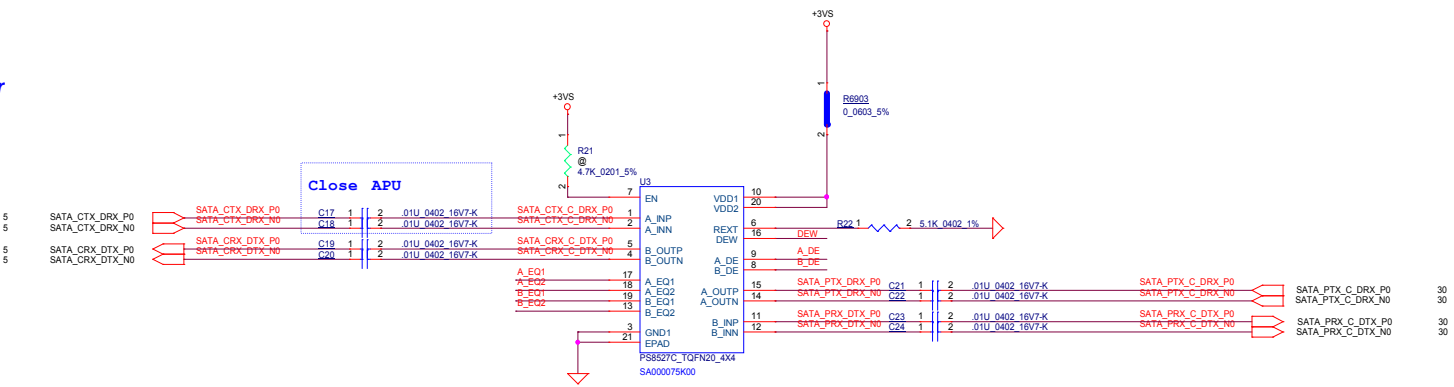


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		2019/06/01			
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Date:				Wednesday, January 09, 2019	
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SATA HDD Redriver



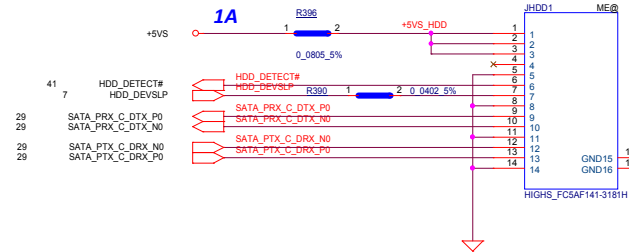
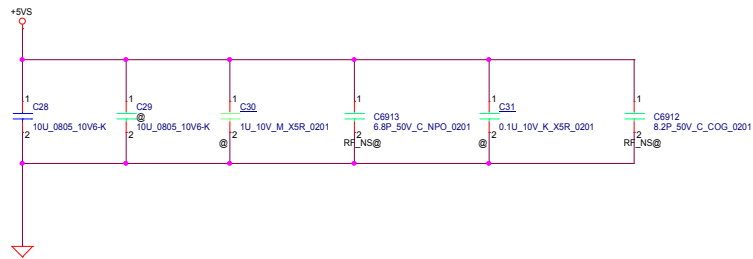
Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
(x_EQ2, x_EQ1) ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.6dB
L/H: for channel loss up to 14.6dB
M/M: for channel loss up to 12.3dB (default)
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.3dB
H/H: for channel loss up to 5dB


De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
(x_DE) ==
M: -3.5dB (default)
L: 0dB
H: -6dB

De-emphasis width adjustment, internally pulled down
(DEW) ==
M: for SATA3 (default)
L: for SATA3
H: for SATA2

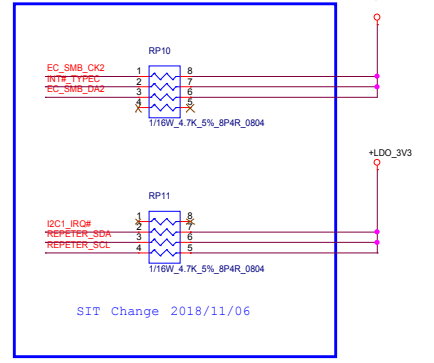
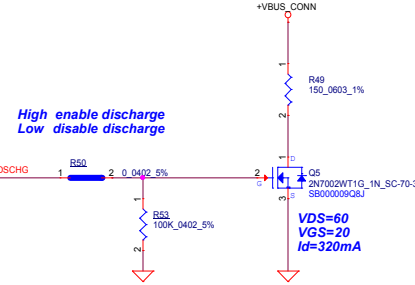
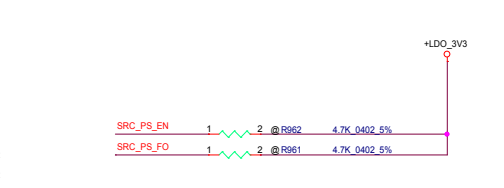
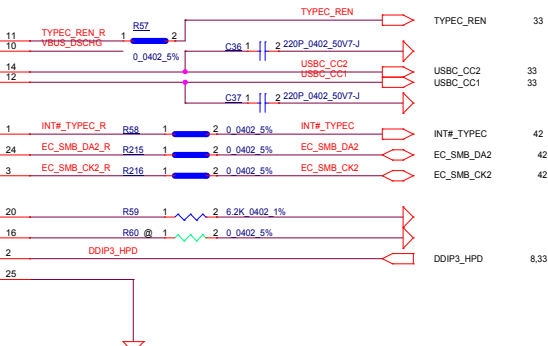
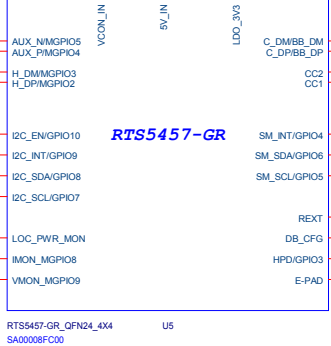
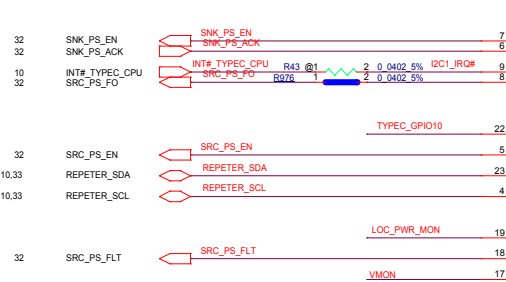
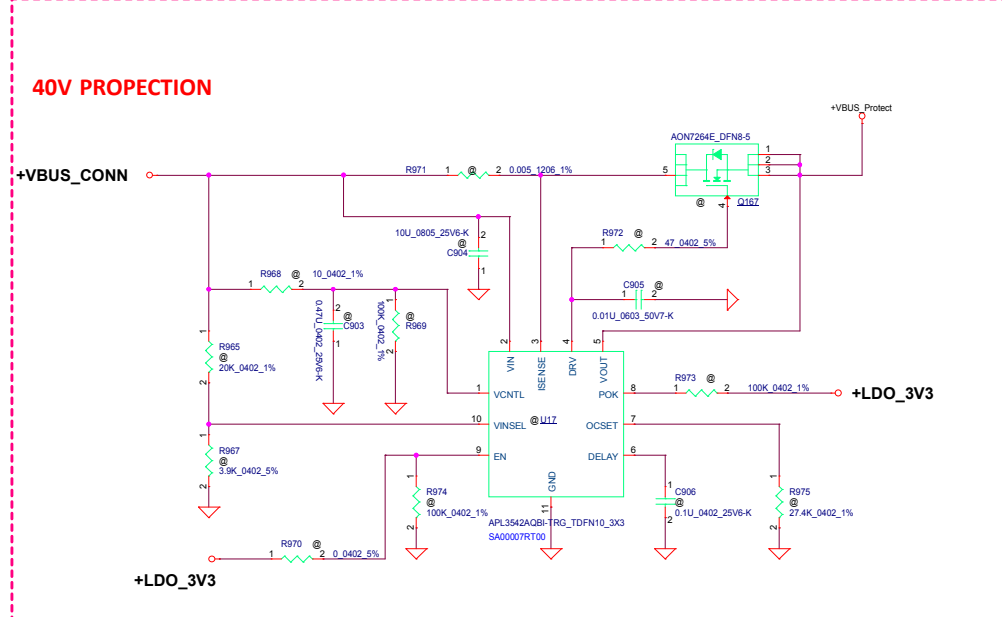
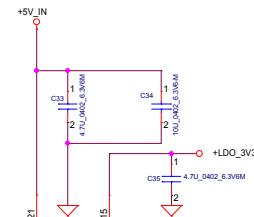
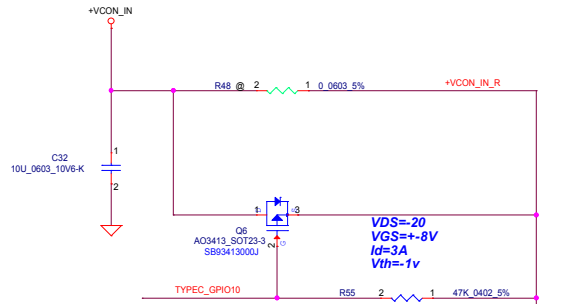
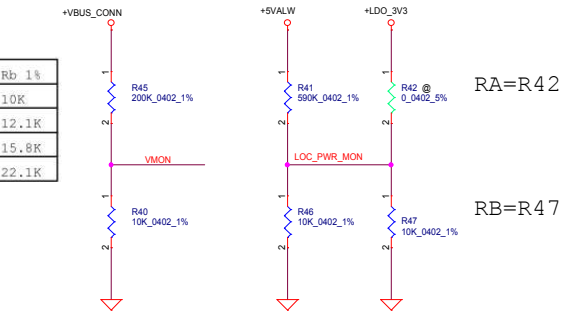
Follow Vendor suggest

SATA HDD CONN.

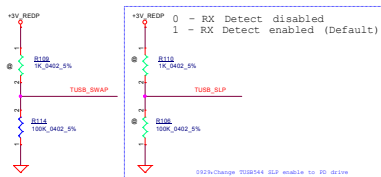
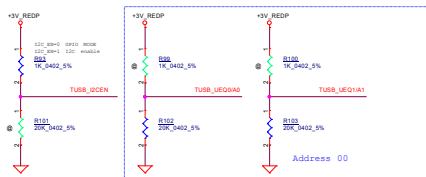
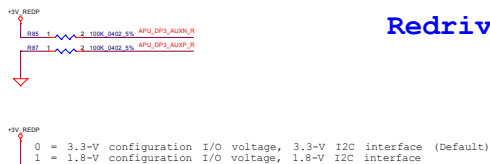


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Issued Date	2018/03/26	Deciphered Date	2019/06/01	SATA HDD	
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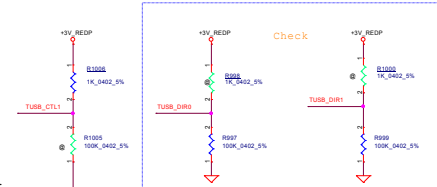
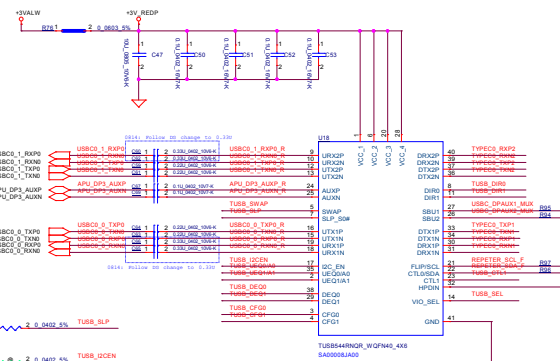
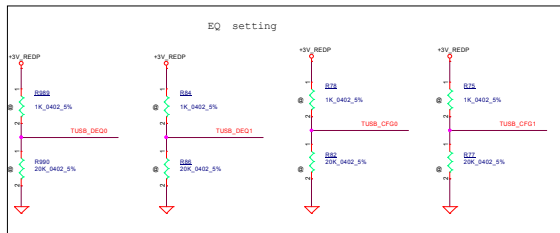
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



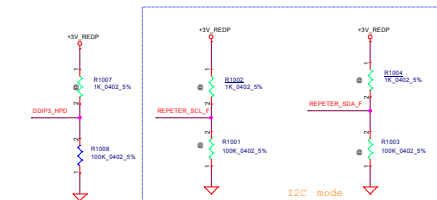
Redriver IC



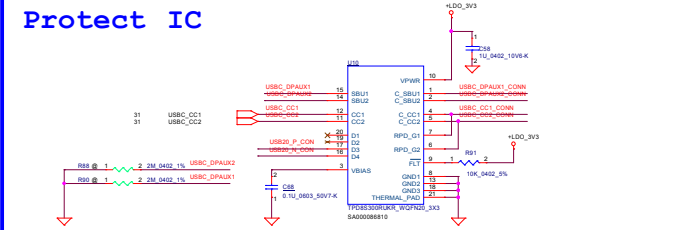
0 - Do not swap channel directions and EQ settings (Default)
1 - Swap channel directions and EQ settings



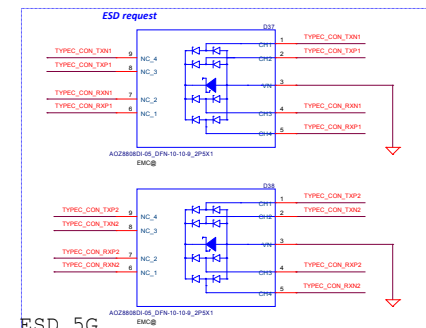
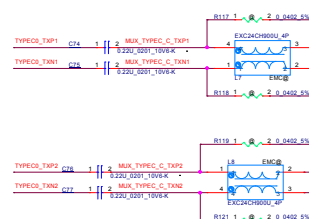
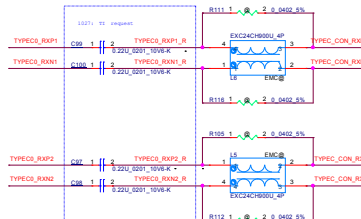
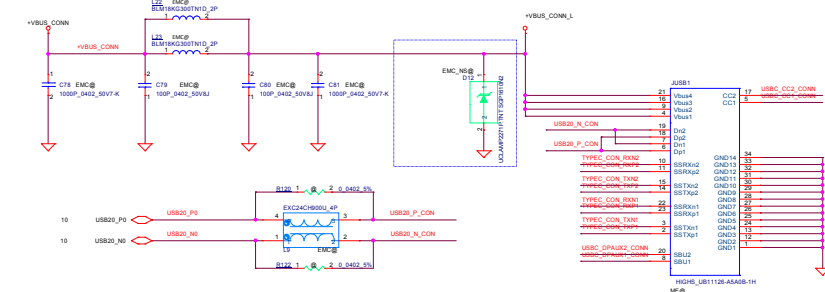
L = DisplayPort Disabled.
H = DisplayPort Enabled.
When I2C_EN = 0, this pin is not used by device.



Protect IC



Type C Connector





On Board (LEFT-Front)

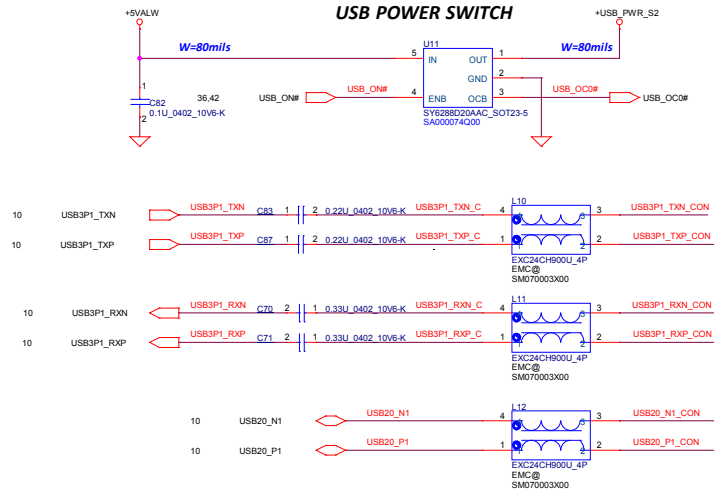
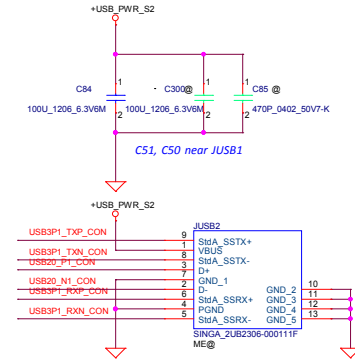
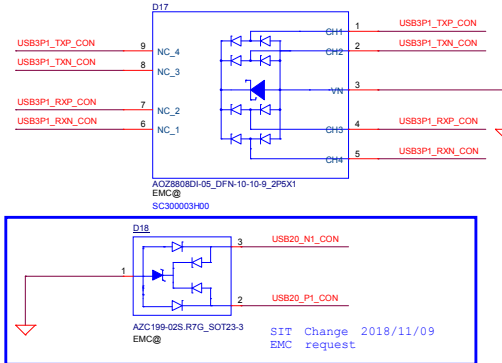
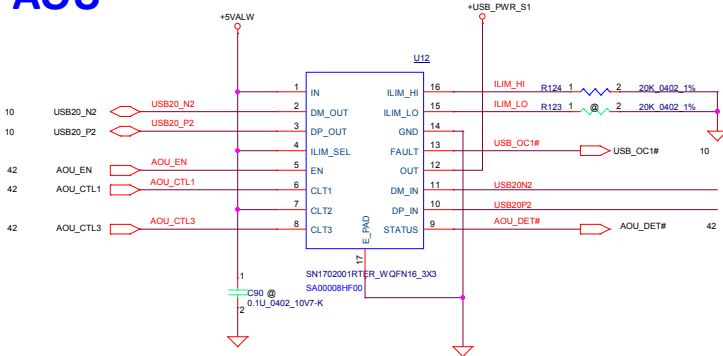


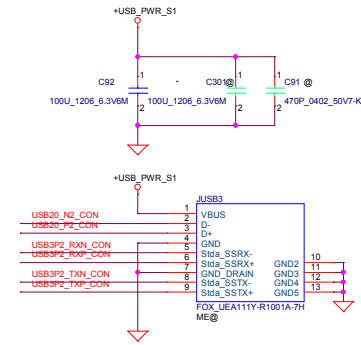
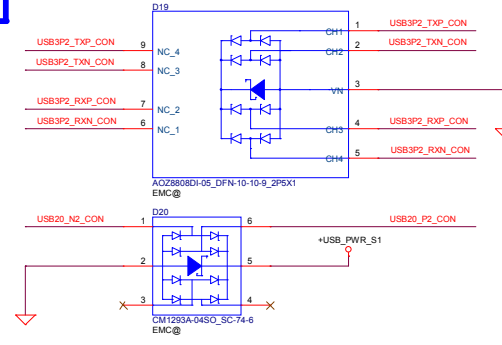
TABLE of POWER SWITCH (U11)		
Vendor	LCFC P/N	Description
SILERGY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T11U SOT-23 5P POWER SWITCH



AOU



On Board (LEFT-Back)



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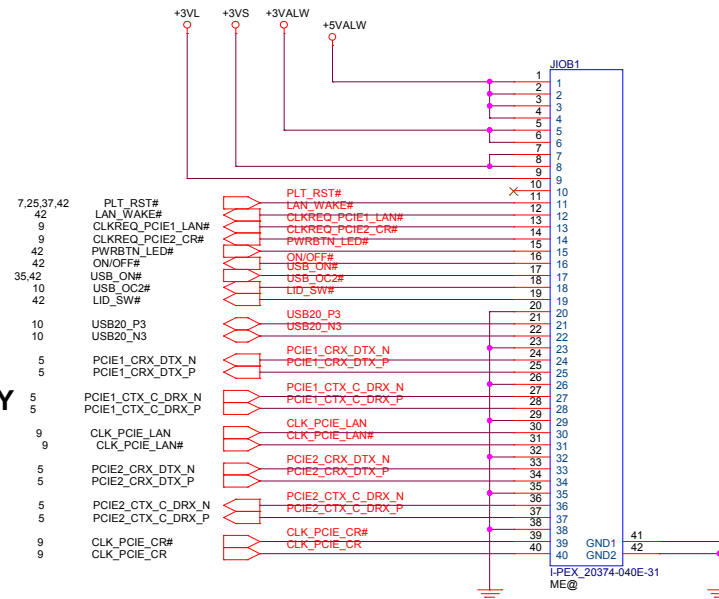
Title		USB3 P1/2 CONN.	
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IO_40_Pin conn

USB2.0

GBE LAN PHY

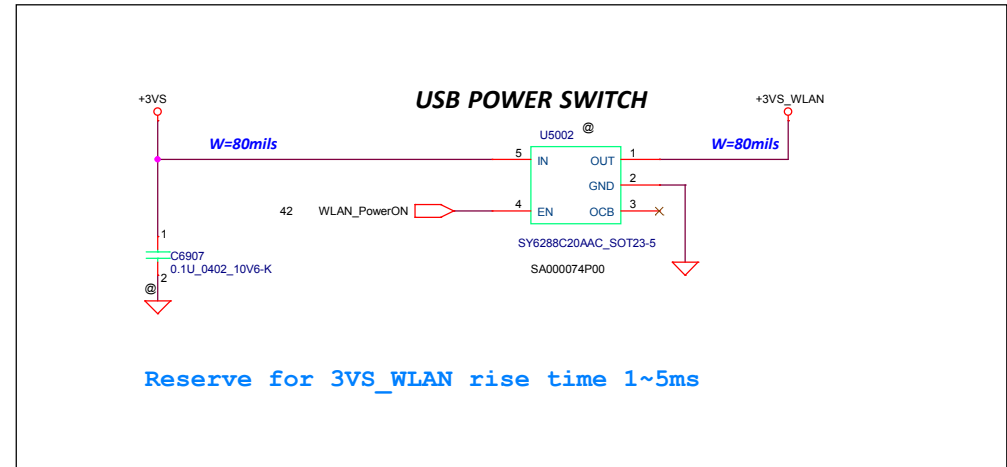
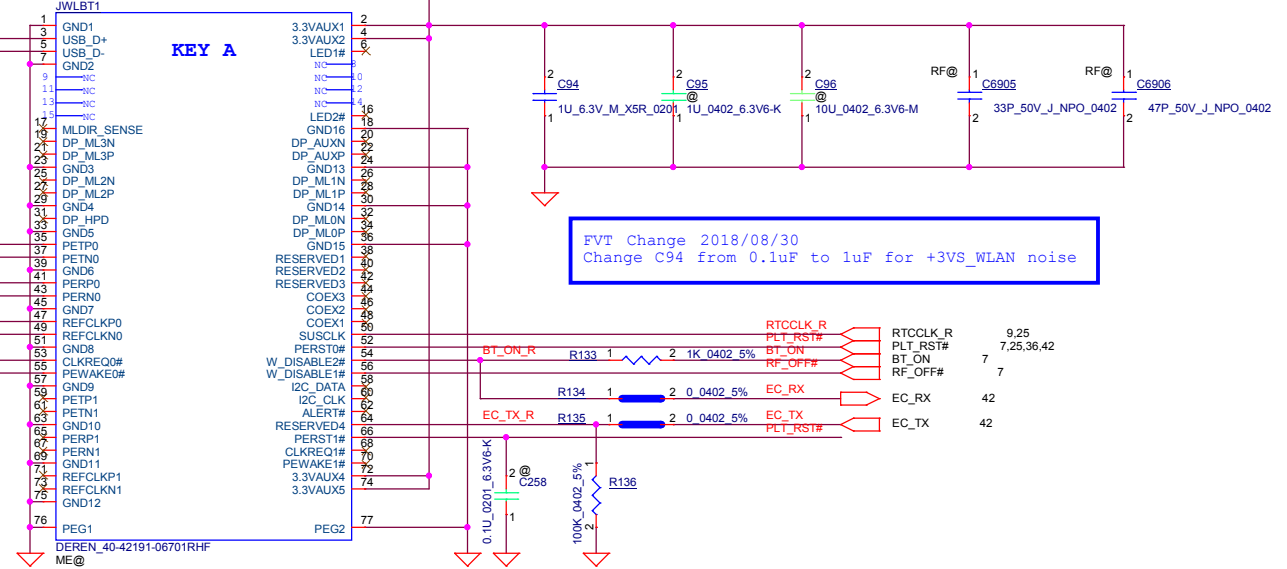
Card Reader

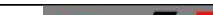


TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR

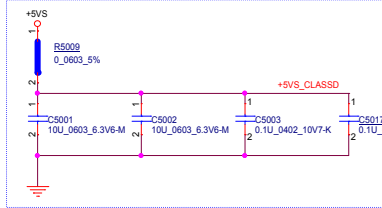
KEY A



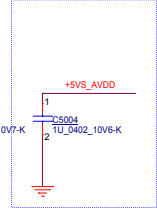
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/03/26	Deciphered Date	2019/06/01	M.2 SOCKET 1 WLAN	
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+5VS ○ ○ ○ +5VS 28,30,39,46,48,51
 +3VL ○ ○ ○ +3VL 31,36,42,52,55,57
 +3VALW ○ ○ ○ +3VALW 7,8,9,10,12,26,33,36,37,41,42,44,46,47,51,57,58,64

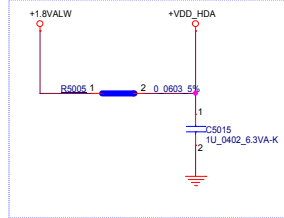
Close to Pin13,16,29



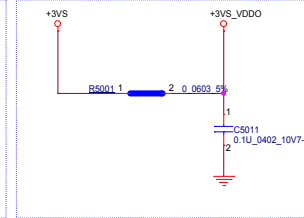
Close to Pin29



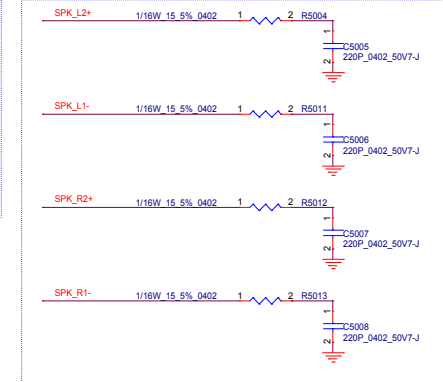
Close to Pin3



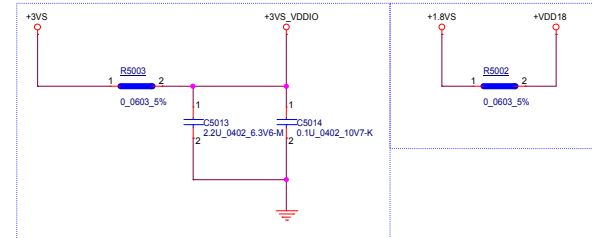
Close to Pin7



EMI filter for Class D output signals
 Close to Codex

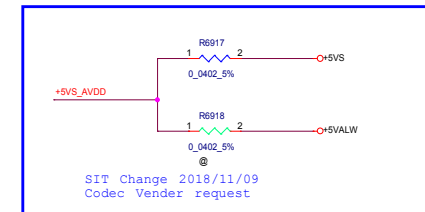
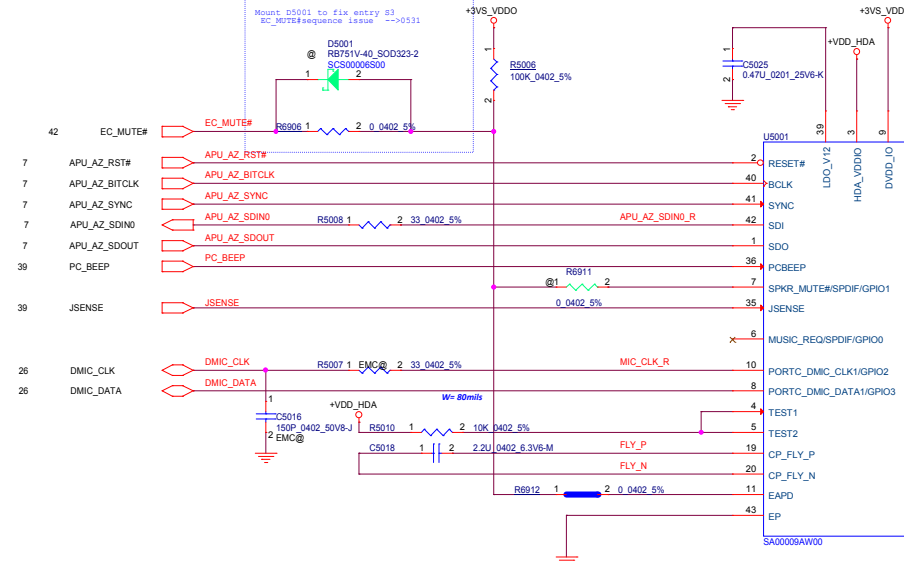


Please Close to Pin9



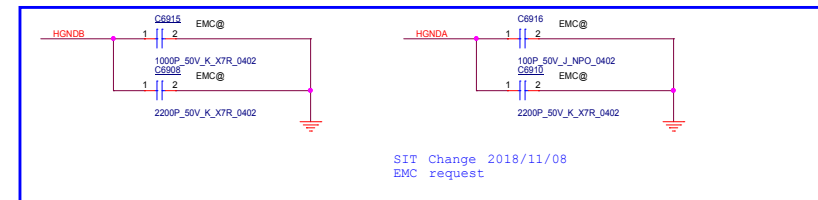
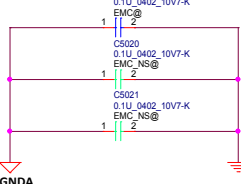
Mount D5001 to fix entry B3
 EC_MUTE#sequence issue -->0531

D5001
 RS751V40_S0D323-2
 SC500006500



SIT Change 2018/11/09
 Codex Vender request

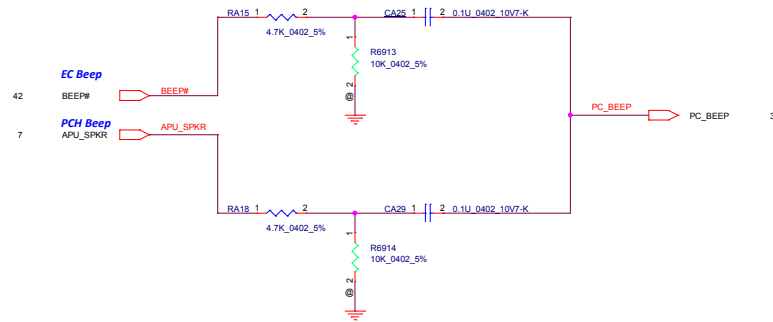
W= 300mils



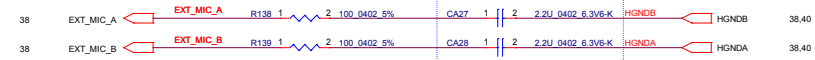
SIT Change 2018/11/08
 EMC request

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PC Beep

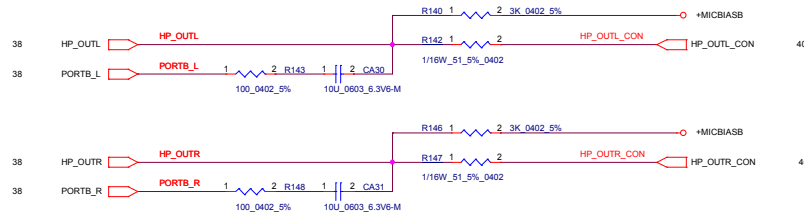


EXT. MIC/LINE IN Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A

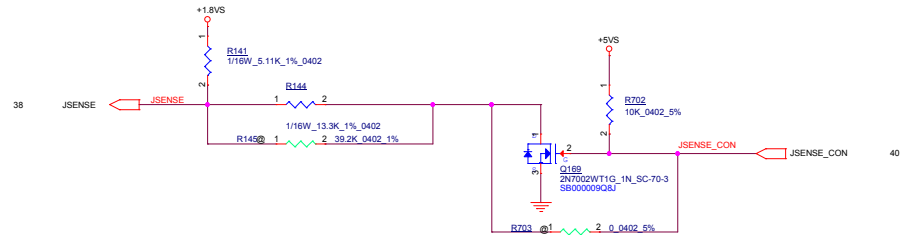


Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

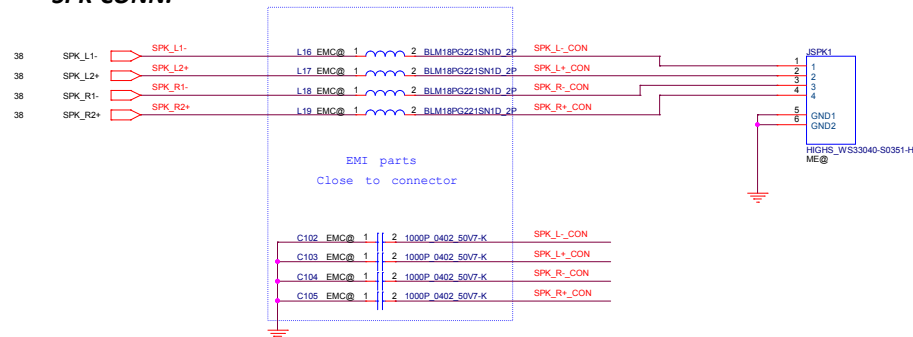
HeadPhone/LINE OUT

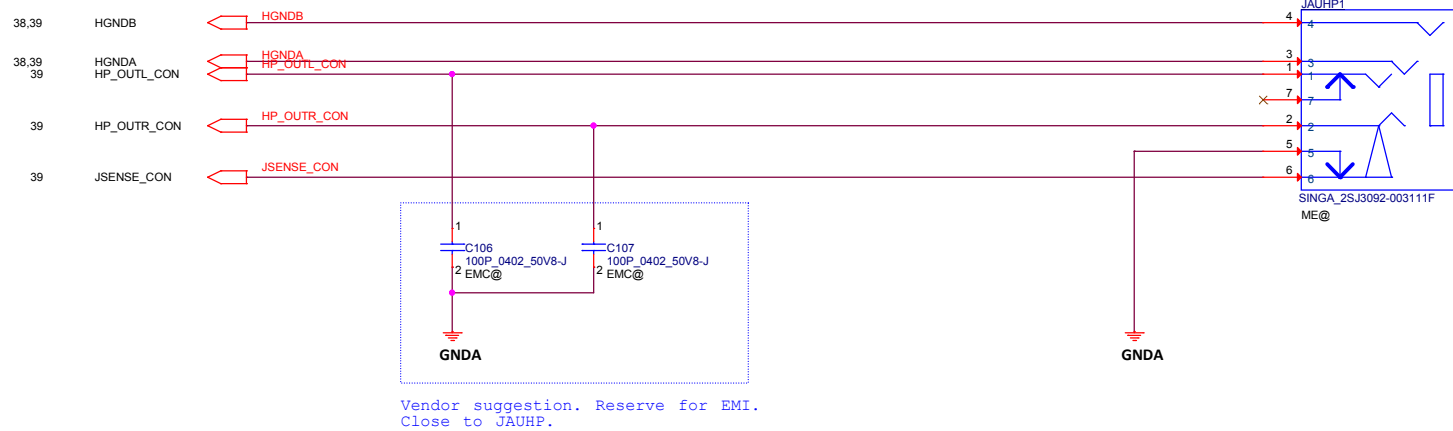


CA31, CA32 change to 4.7uF for Quality requirement

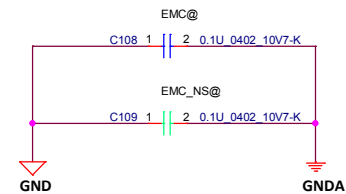
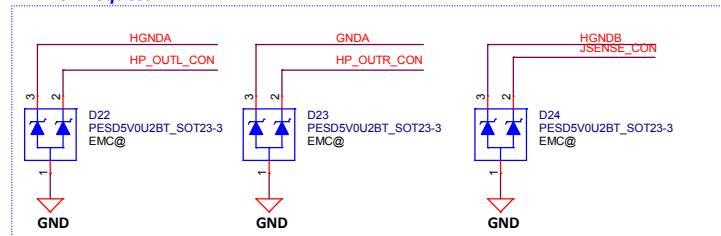


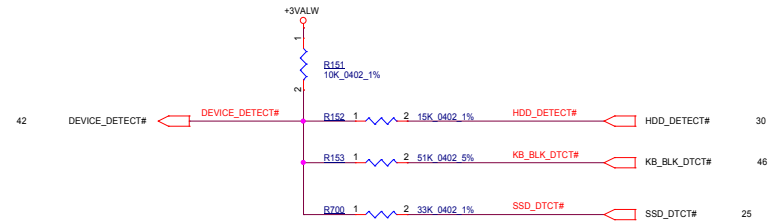
SPK CONN.





ESD request



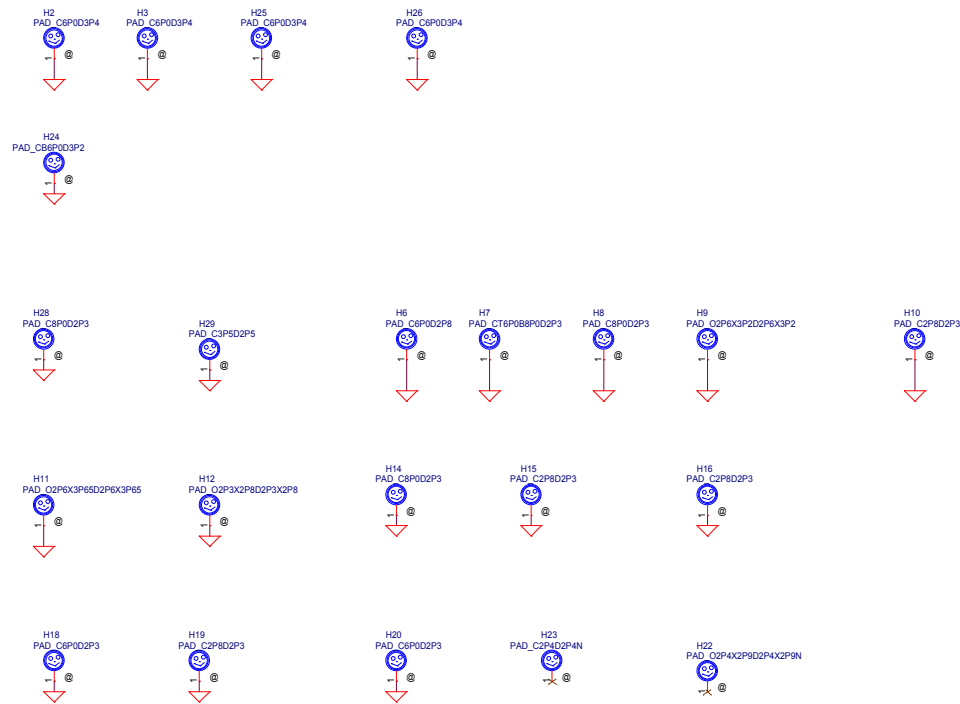


Vcc	3.3V					
R151	10K +/- 5%					
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V
HDD_DETECT#	V	V	V	X	X	X
KB_BLK_DTCT#	X	V	X	X	V	X
SSD_DTCT#	X	X	V	V	X	X

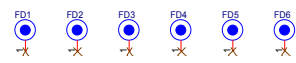
CPU

WLAN

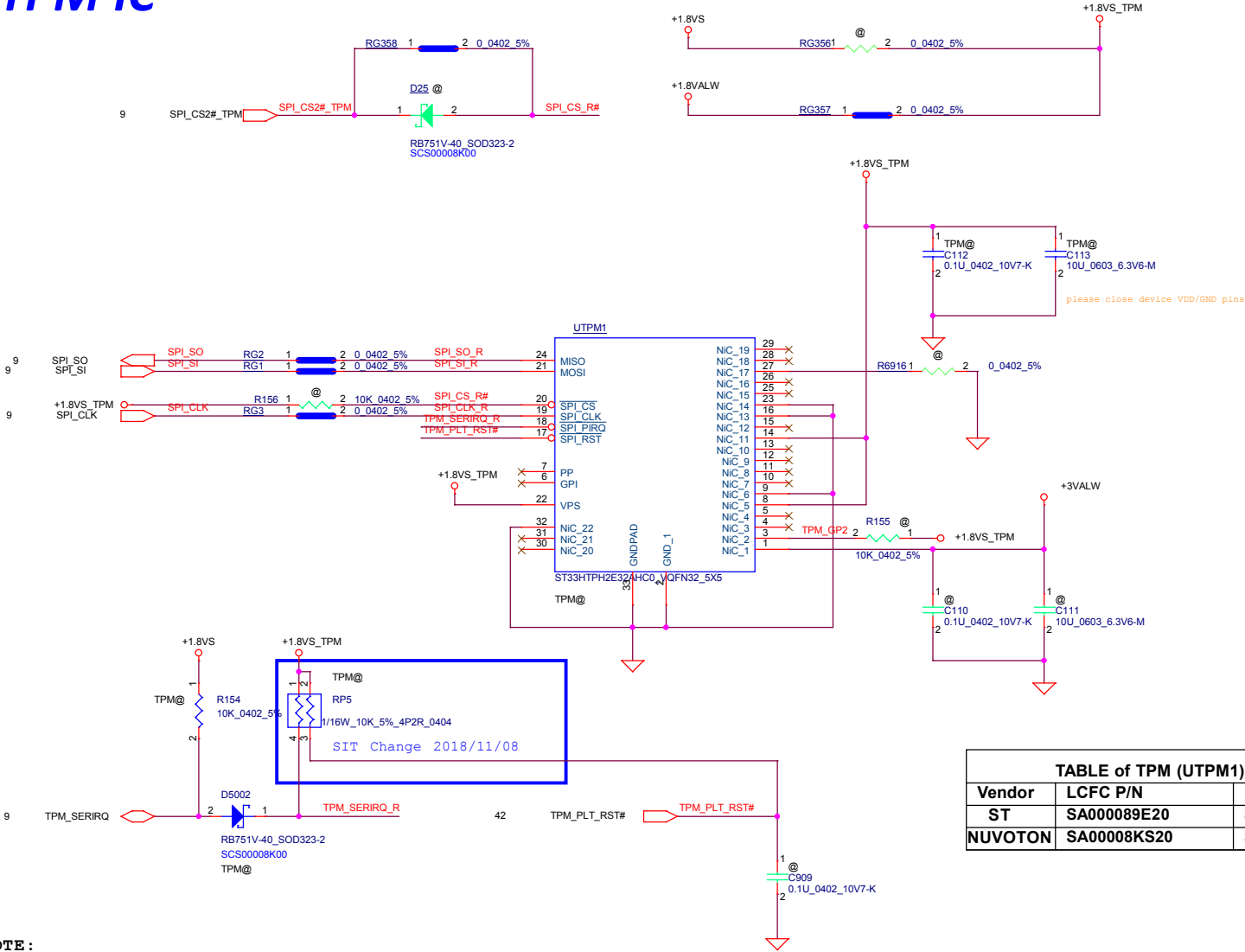
Screw Hole



PCB Federal Mark PAD



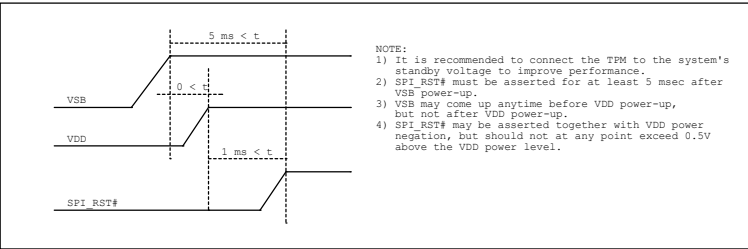
TPM IC



Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HPTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	SPI_PIRQ#	SPI_PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	CS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

TABLE of TPM (UTPM1)		
Vendor	LCFC P/N	Description
ST	SA000089E20	S IC ST33HPTPH2E32AHC0 VQFN 32P TPM 2.0
NUVOTON	SA00008KS20	S IC NPCT750LABYX QFN 32P TPM 2.0 QS/MP

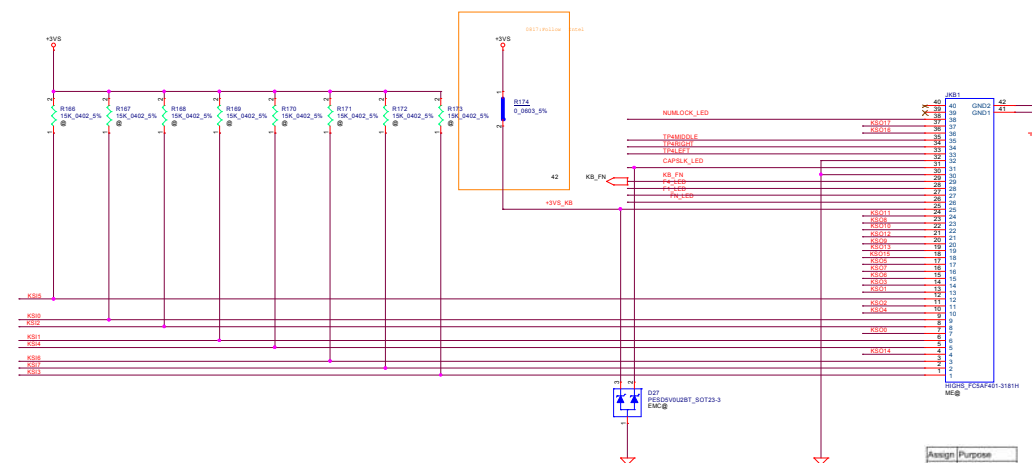
NOTE:
Check timing sequence in SDV phase.



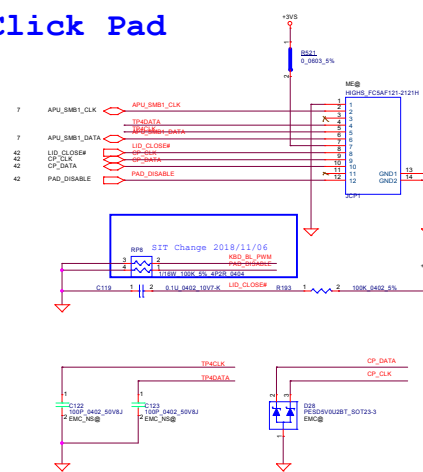


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				<small>Custom C</small>	
				<small>Date: Wednesday, January 09, 2019</small>	
				<small>Sheet 45 of 55</small>	
				<small>Rev</small>	
				<small>0.1</small>	
				JINN/DOOKU 2.0	

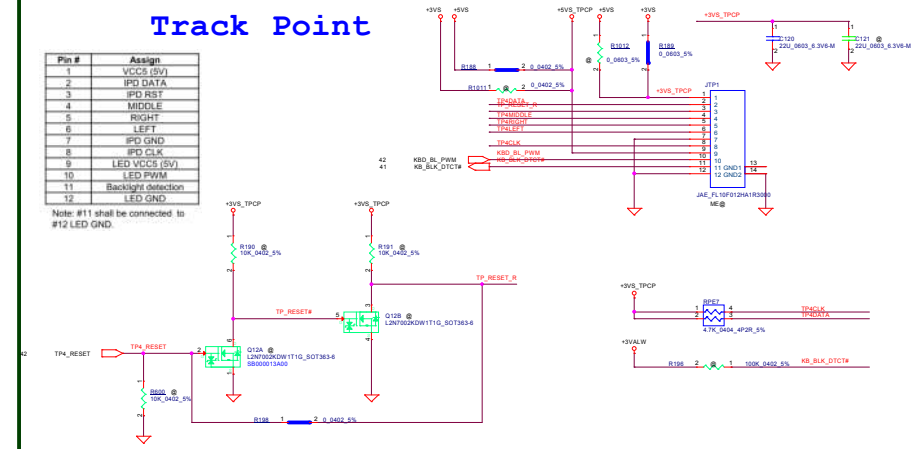





Pin #	Assign
1	SENSE5
2	SENSE6
3	SENSE7
4	DRV14
5	SENSE8
6	DRV0
7	SENSE9
8	SENSE2
9	SENSE5
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV8
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV19
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKE
30	GM
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

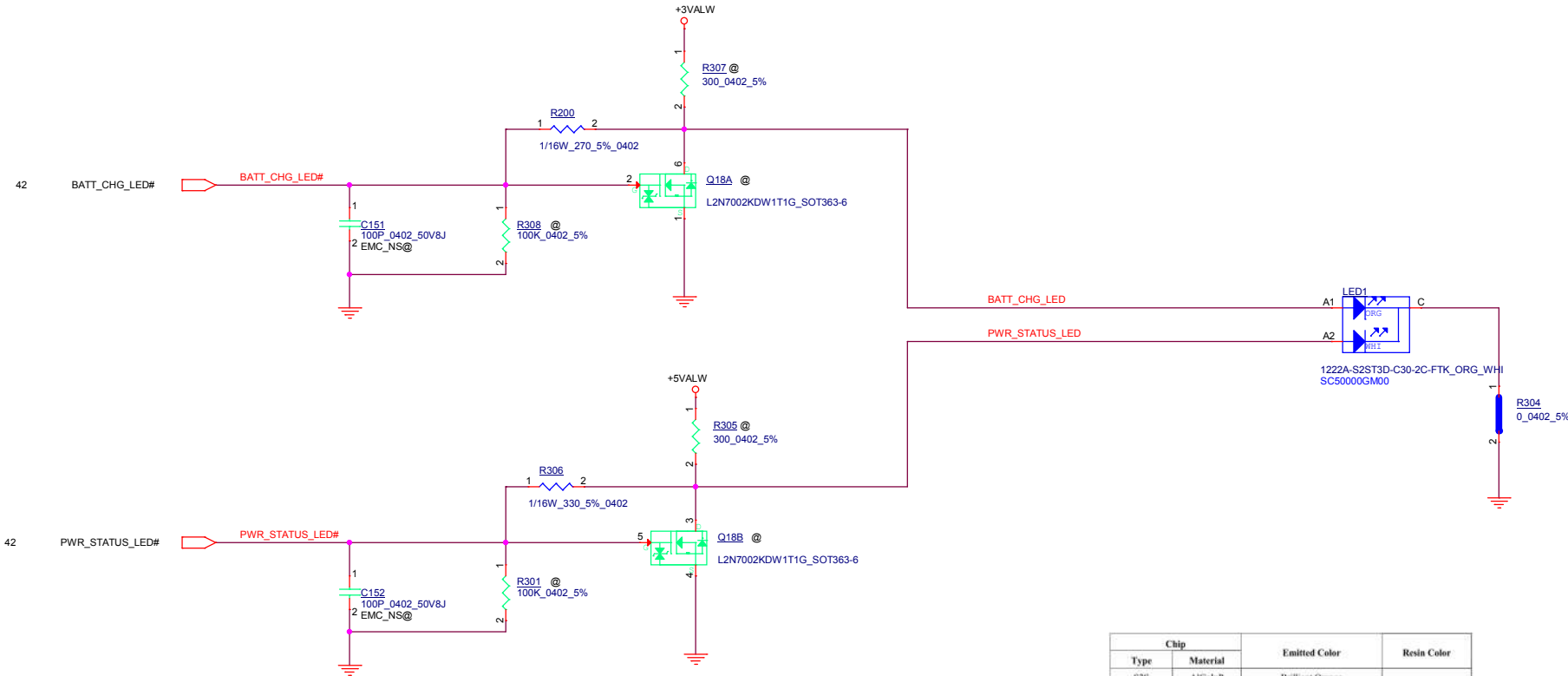


Pin #	Assign
1	VCC5 (5V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND



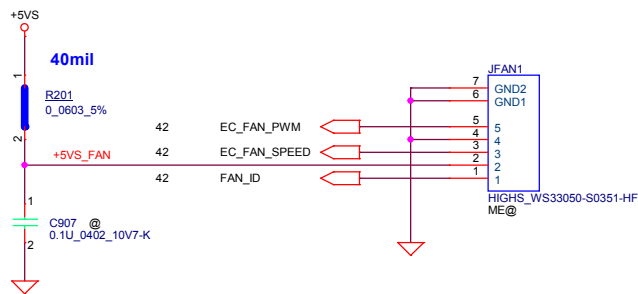
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Size	A		Scale	1/4" = 1'-0"	
Date	Wednesday, January 16, 2019		Drawn	JIN/DOOKU 2.0	

POWER ADAPTER Bi-COLOR (ORANGE/WHITE)



Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

FAN CONN.



Thermal Sensor

1 Near

2 Remote

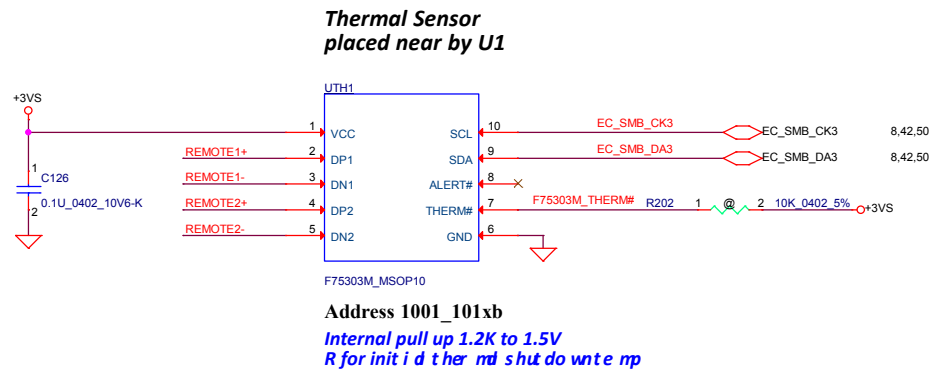
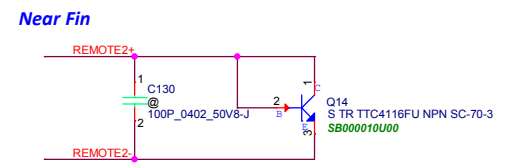
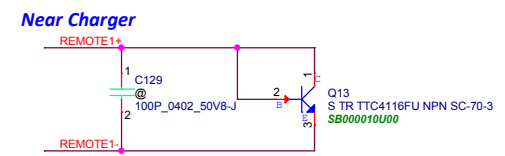
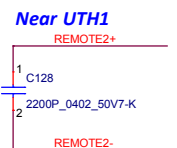
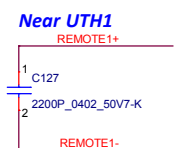


TABLE of Thermal Sensor (UTH1)		
Vendor	LCFC P/N	Description
FINTEK	SA000046C0J	S IC F75303M MSOP 10P SENSOR

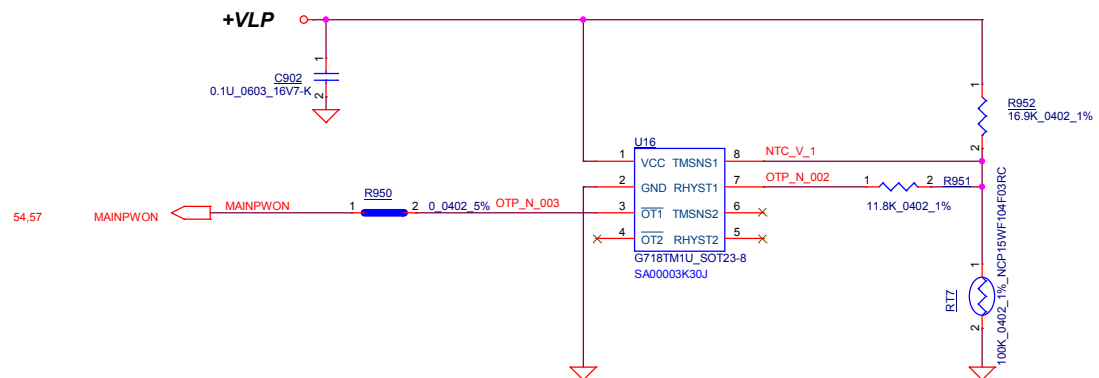


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:

Trace width/space:10/10 mil

Trace length:<8"

HW Protect



over temperature threshold:

RSET=3*RTMH

100+/-30C

Hysteresis temperature threshold.

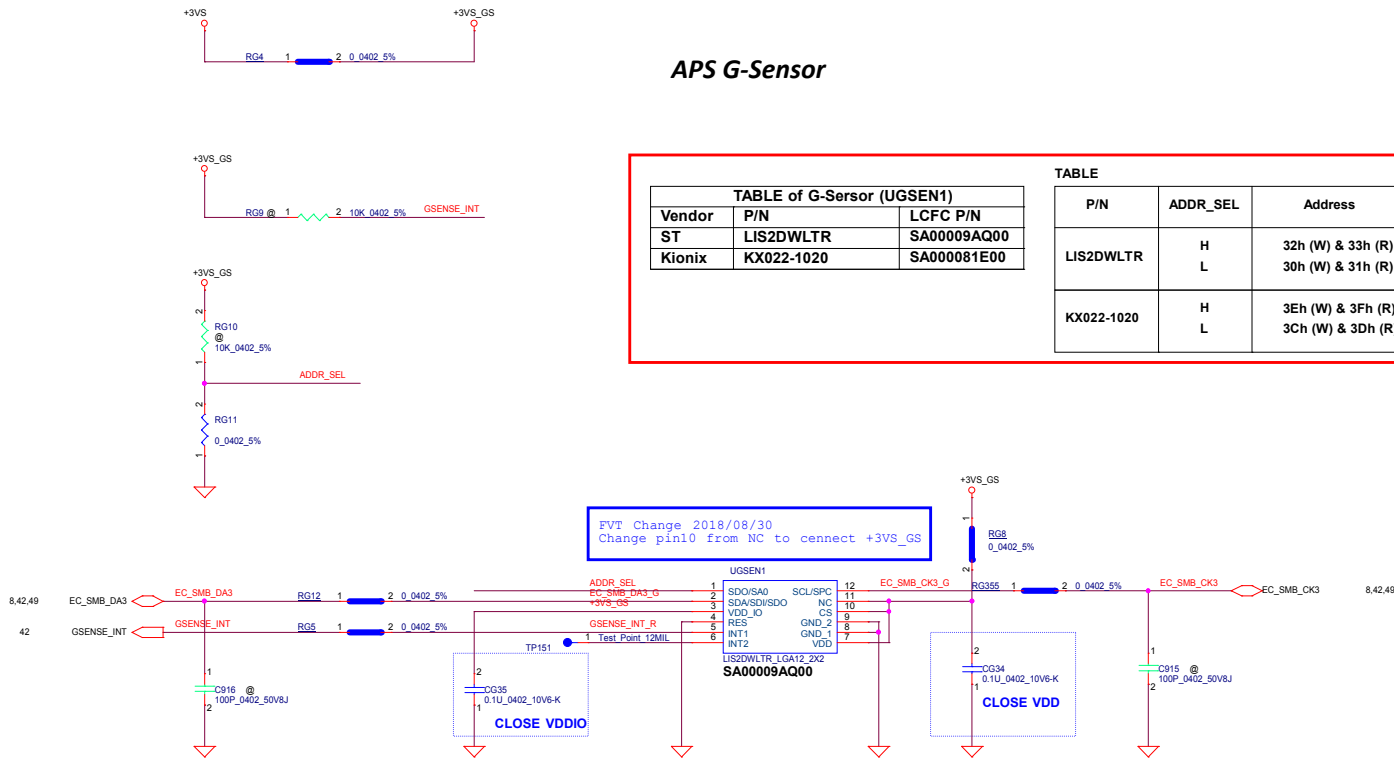
RHYST=(RSET*RTML) / (3*RTML-RSET)

80+/-30C

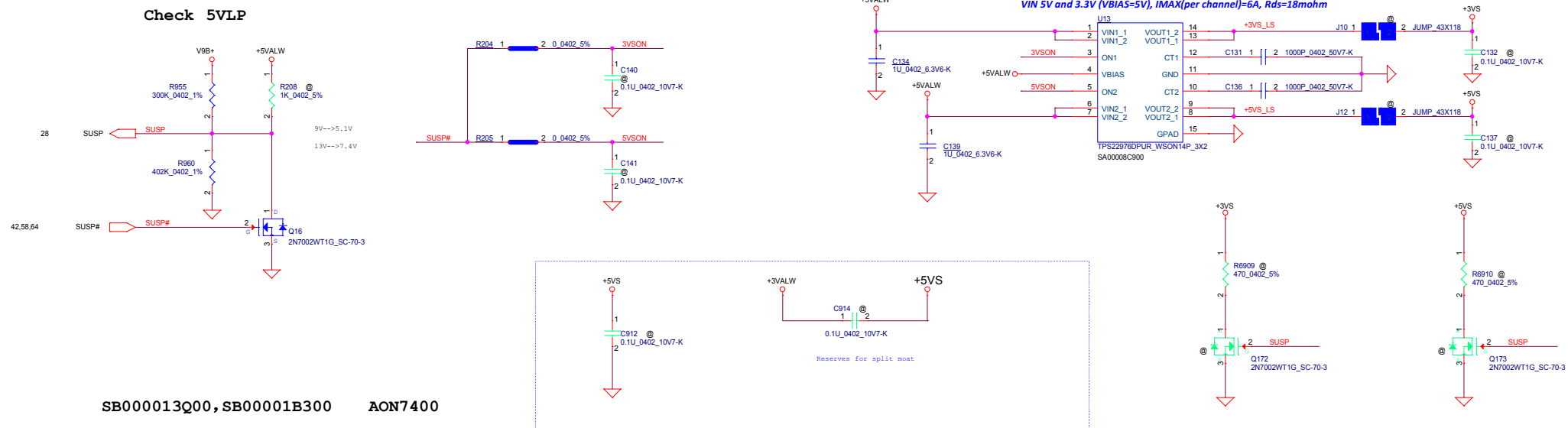
APS G-Sensor

TABLE of G-Sensor (UGSEN1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00

TABLE		
P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

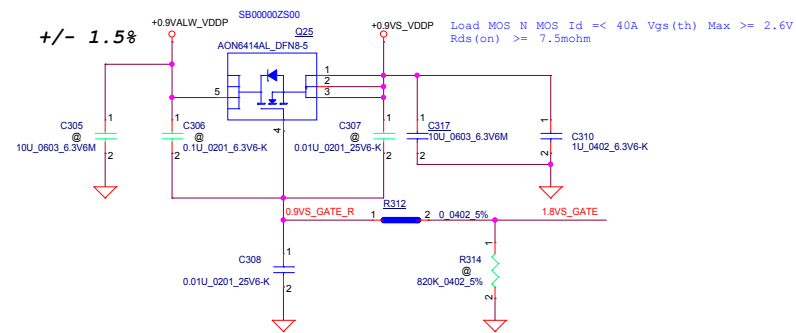


+3/5VS load Switch

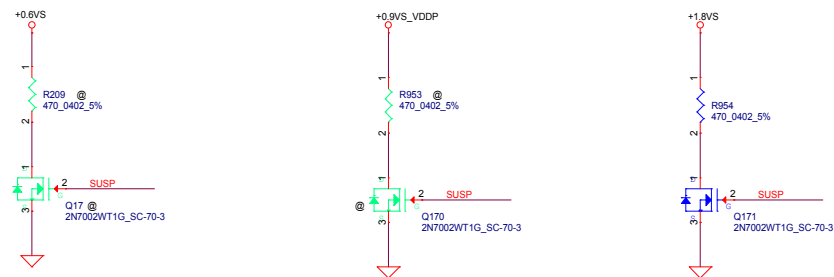


+VDDP load Switch

+0.9VALW_VDDP to +VDDP 10A request
V9B+ 9V--13V



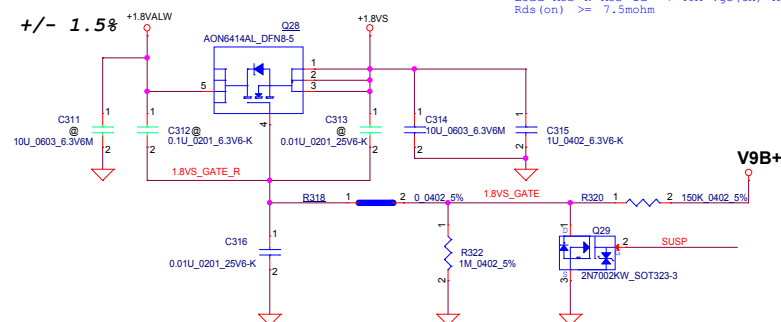
For DisCharge




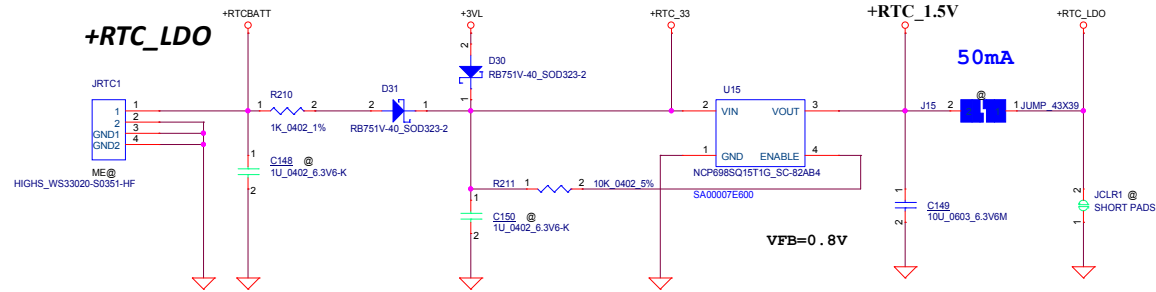
+1.8VS load Switch


+1.8VALW to +1.8VS 2A request

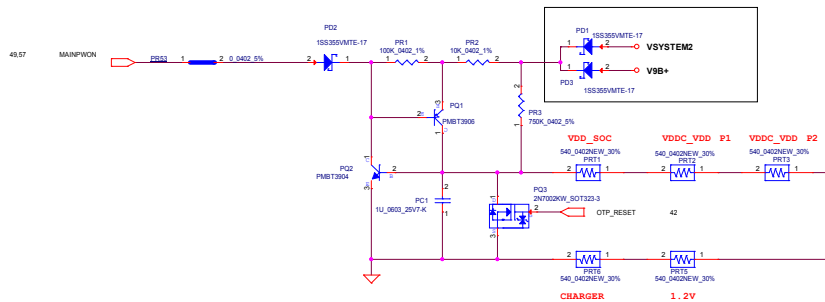
Load MOS N MOS Id =< 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

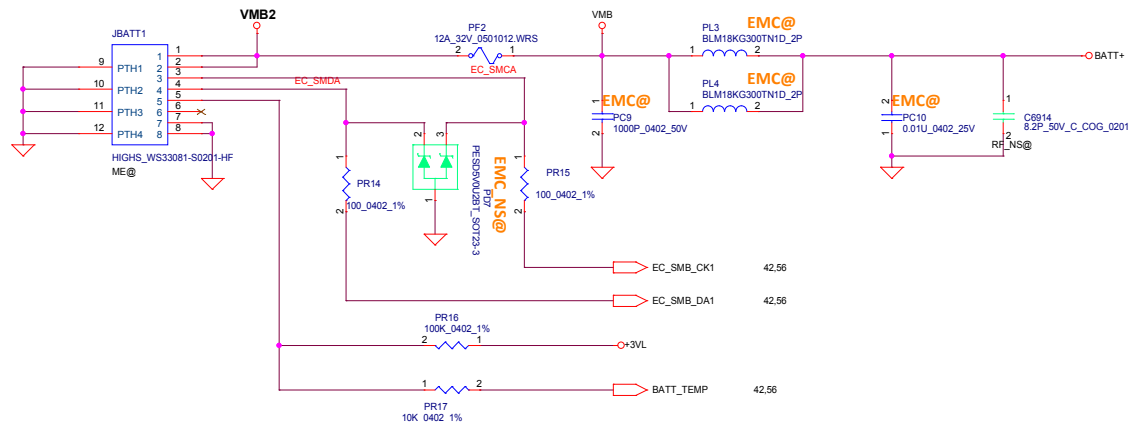


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Custom						0.1
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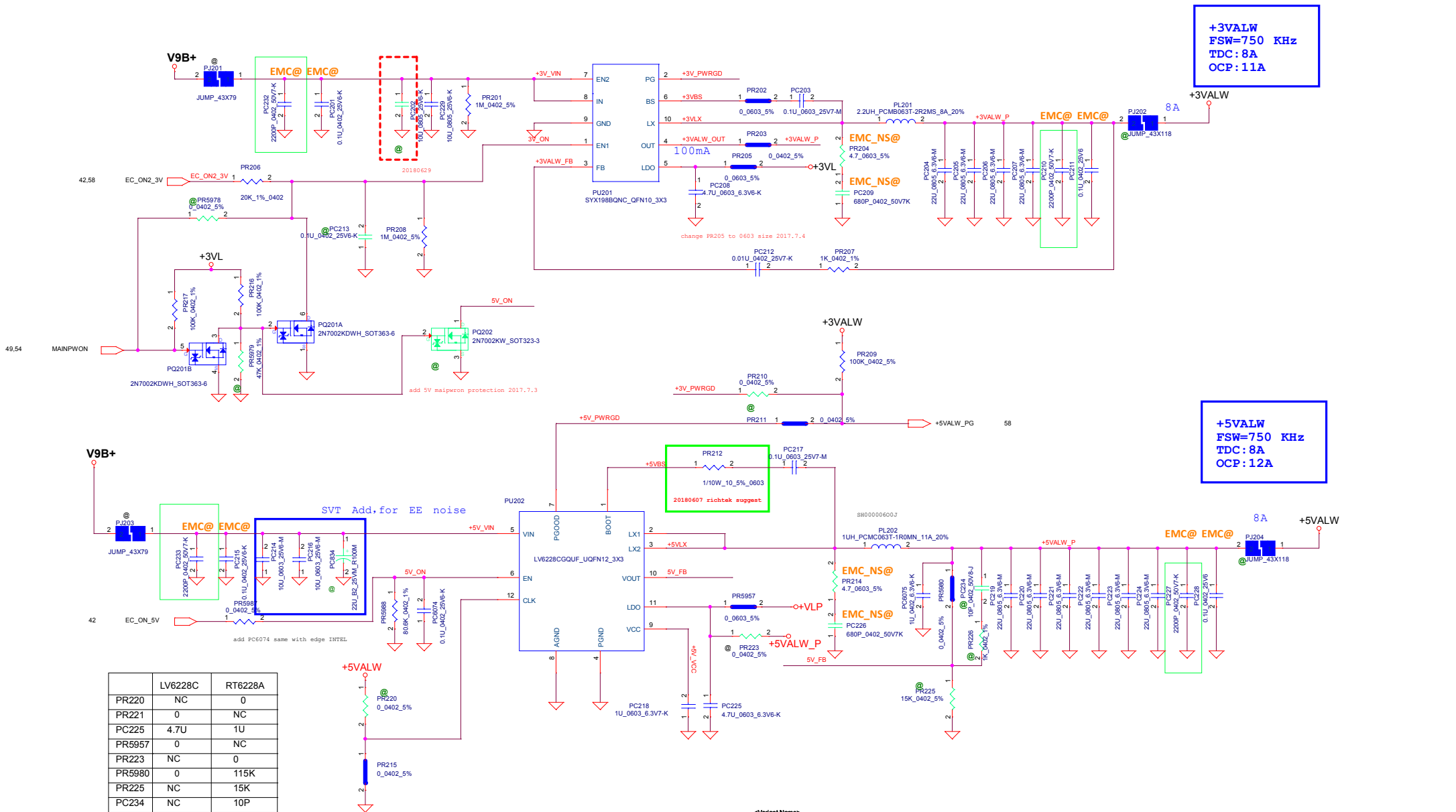
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					Date: Wednesday, January 09, 2019
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2018/03/26

Deciphered Date

2019/06/01

Title

3VALWP/5VALWP

Size

Custom

Document Number

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Date

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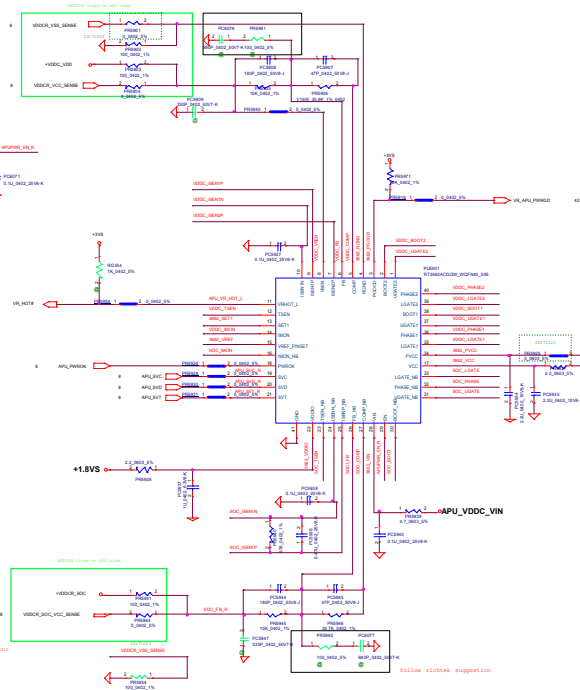
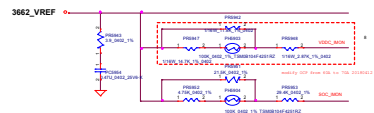
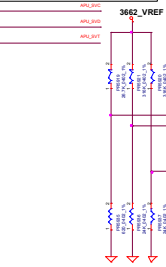
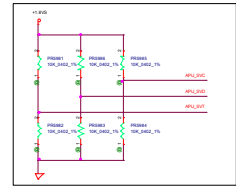
Sheet 57 of 65

Rev

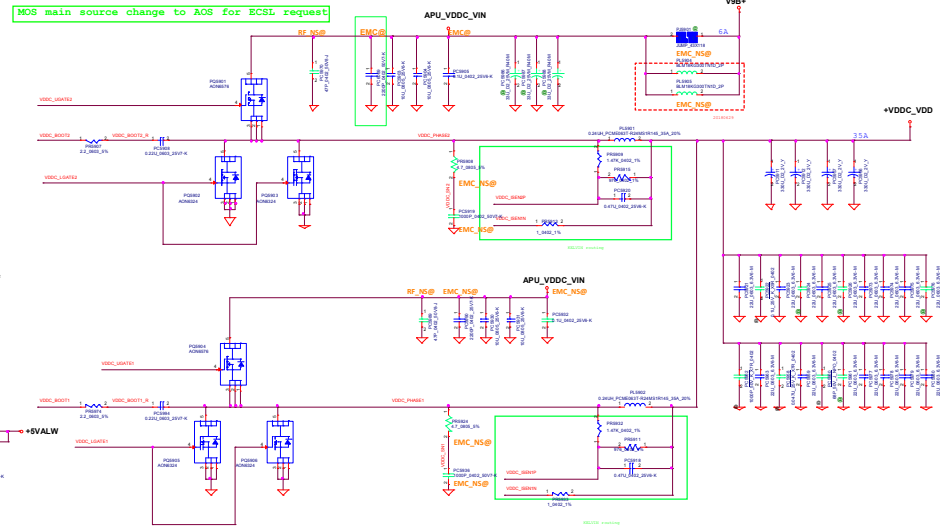
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SVC	SVD	Boot Voltage
0	0	1.1V
1	1	1.0V
1	0	0.9V (default)
1	1	0.8V

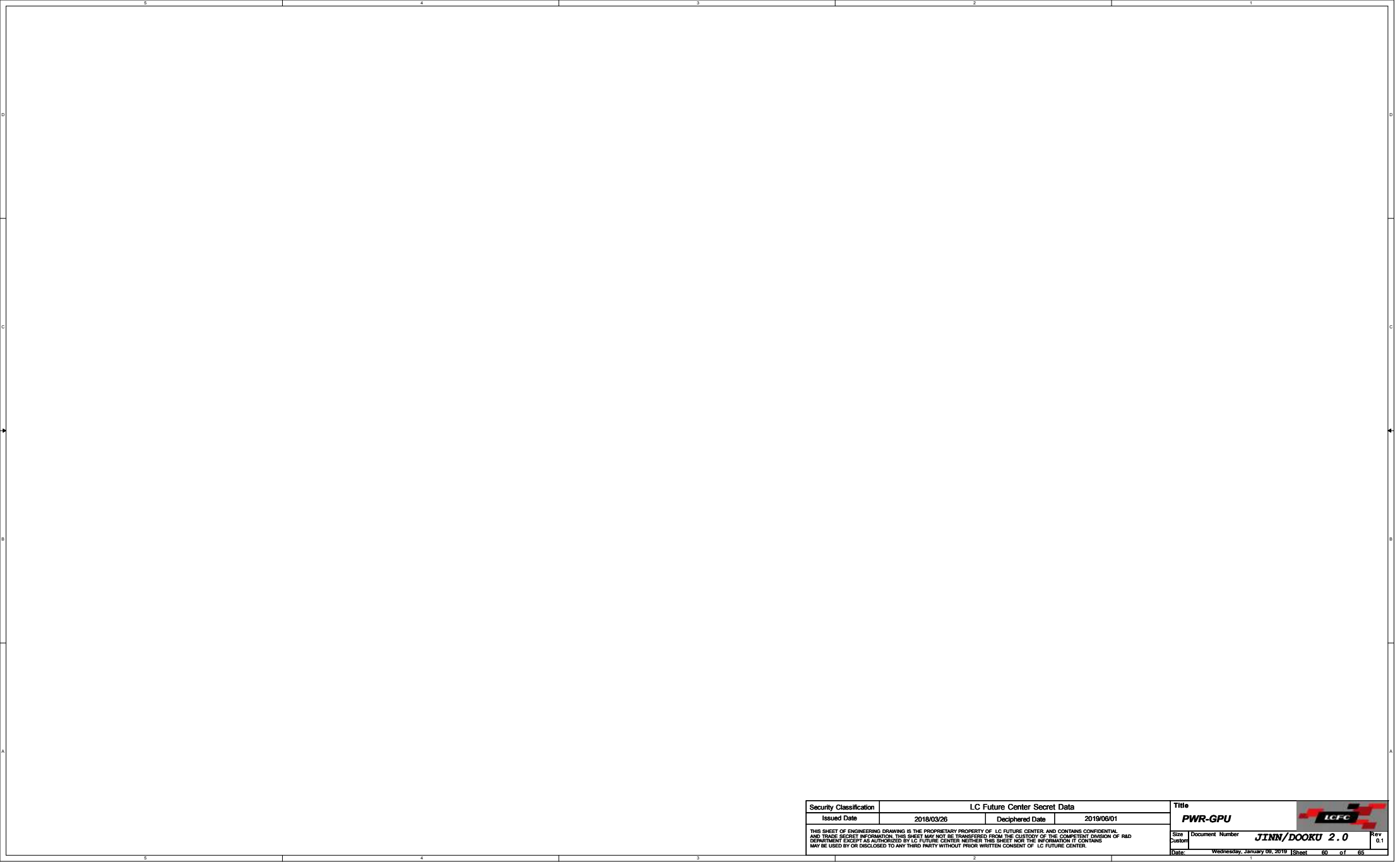


MOS main source change to AOS for ECSEL request




VDDC_VDD
FSW=300kHz
Slew rate: 12.5mV/us
TDC=50A EDC=45A
OC=15A
OVP=1.8V
Load: Line=2mhm
Ripple=+/-20mV
MAX AC: VDD_VDDC +65mV
MIN AC: VDD_VDDC -60mV


VDDCR_SOC
FSW=300kHz
Slew rate: 12.5mV/us
TDC=10A EDC=13A
OC=15A
OVP=1.8V
Load: Line=2mhm
Ripple=+/-20mV
MAX AC: VDD_VDDC_SOC +70mV
MIN AC: VDD_VDDC_SOC -60mV

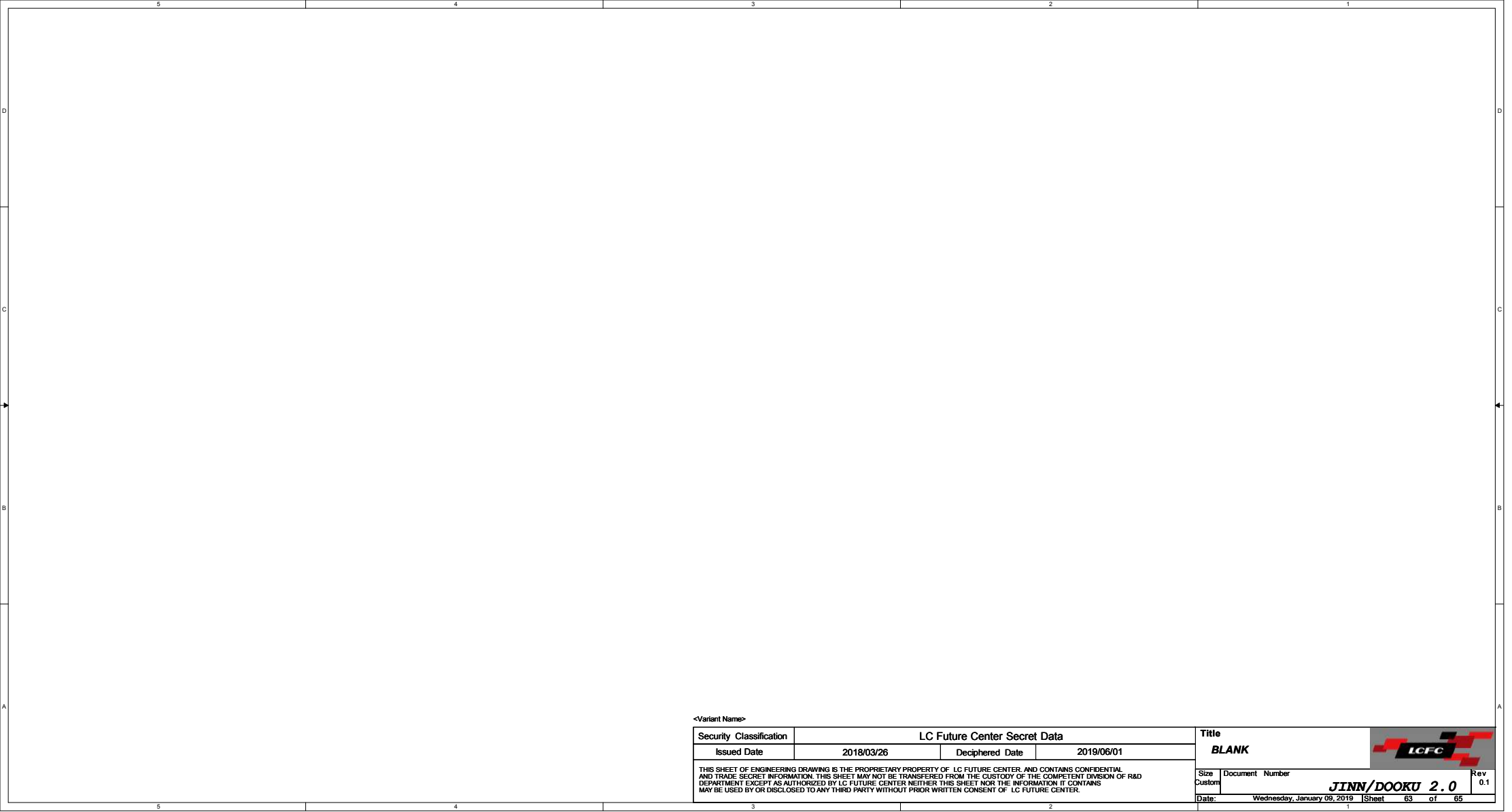


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				<small>Date:</small> Wednesday, January 06, 2019 <small>Sheet</small> 60 <small>of</small> 65	




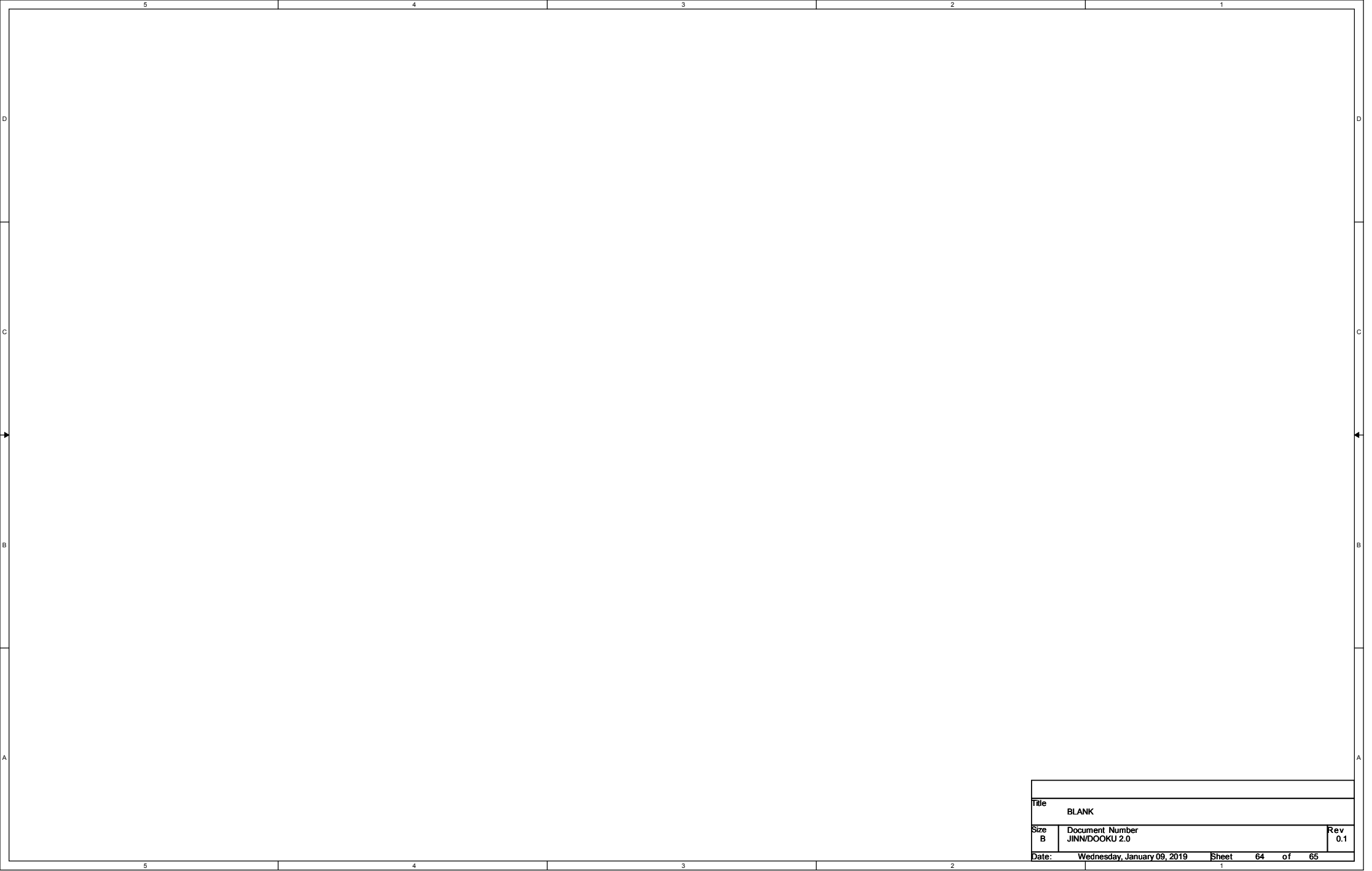
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				Date: Wednesday, January 09, 2019		Sheet 62 of 65	
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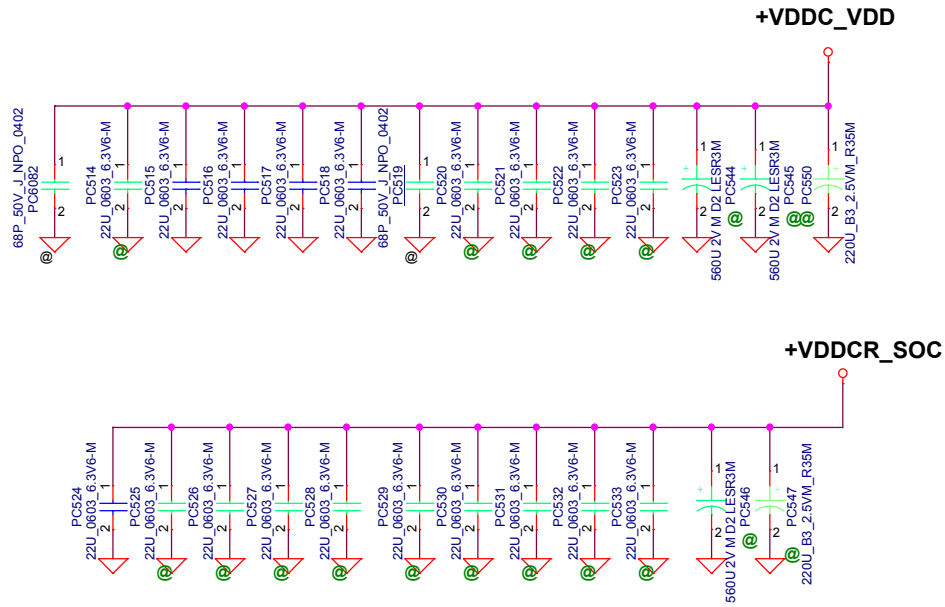


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Date:		Tuesday, January 15, 2019		Sheet 65 of 65					